

Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

## POWER



## Layout

### DMI

Differential 85ohm (single 50)  
n,p mismatch <5mils  
maximum mis-match between inter-pairs :  
7000 mils (177.8 mm)  
Max: [ 2000 to 8000 mils, 3vias ]  
436735 Huron River Design Guide 1.0

## Layout

### FDI

Differential 85ohm (single 50)  
n,p mismatch <5mils  
pair to pair mismatch < 7 inches  
Max:  
3vias : 2000 to 8000 mils  
4vias : 2000 to 6500 mils  
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Note:  
FDI ( Flexible Display Interface):  
Carries display traffic  
from the integrated graphics controller  
to the legacy display connectors in the PCH.

## Layout

DP\_ICOMPO :  
Trace Width : 12 mils (0.305 mm)  
To other Signals : 15 mils (0.381 mm)  
Routing Length :500 mils (12.7 mm)

DP\_COMPIO :  
PEG\_RCOMPO  
Trace Width : 4 mils (0.102 mm)  
To other Signals : 15 mils (0.381 mm)  
Routing Length : 500 mils (12.7 mm)

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## Layout

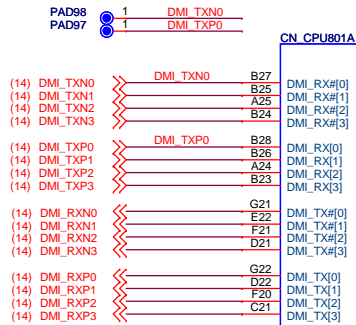
### eDP

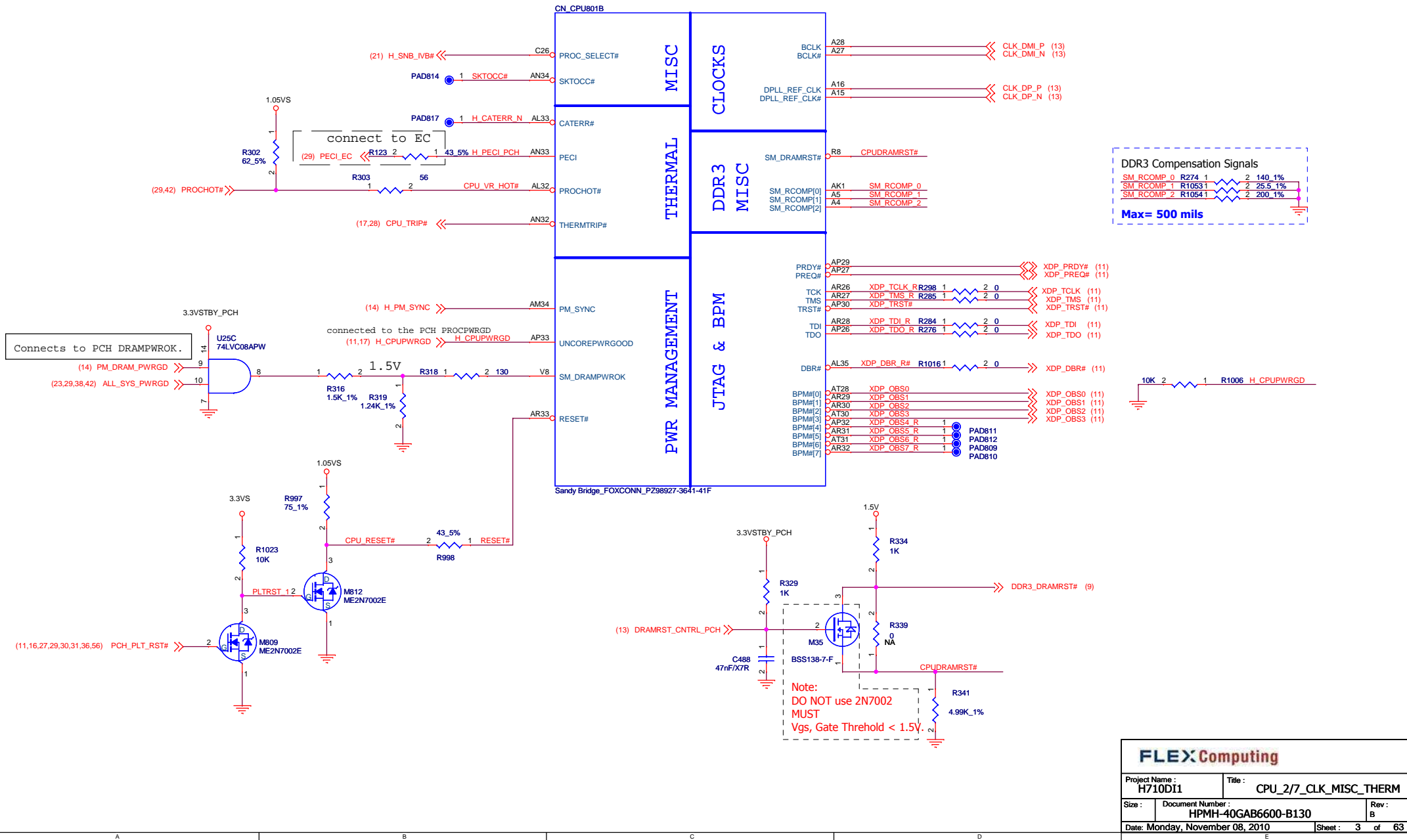
Differential 85ohm (single 50)  
n,p mismatch <5mils  
pair to pair mismatch < 7 inches  
Max:  
2vias : 2000 - 8000 mils  
4vias : 2000 - 8000 mils  
436735 Huron River Design Guide 1.0

## Layout(Switchable Graphics Topology)

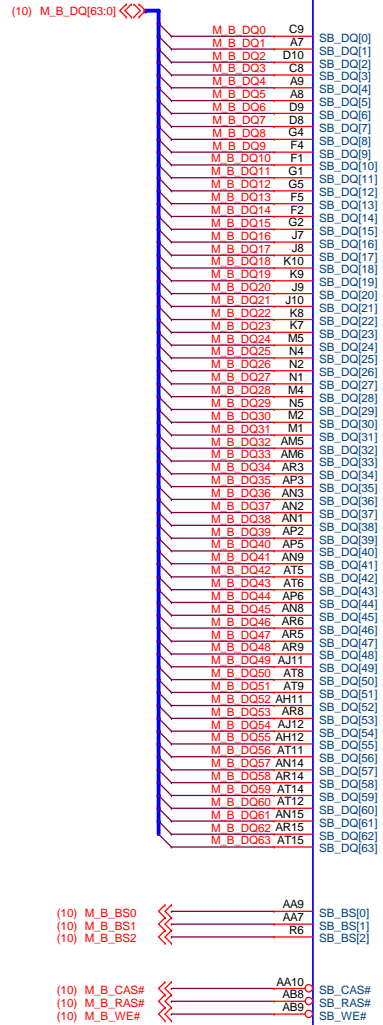
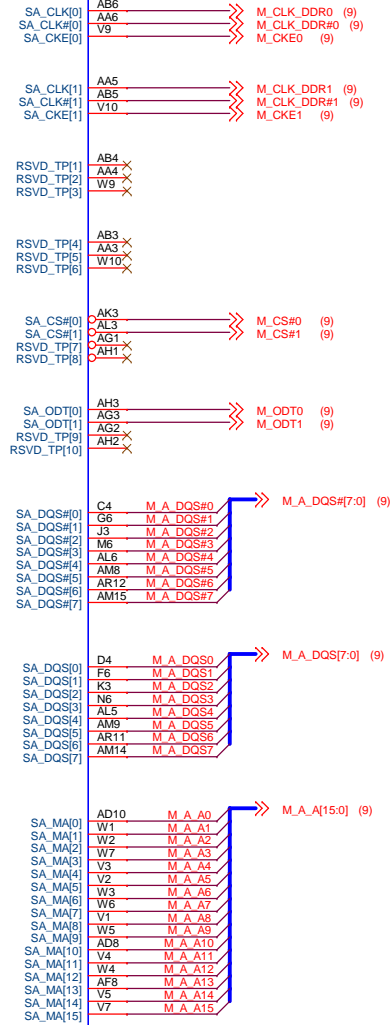
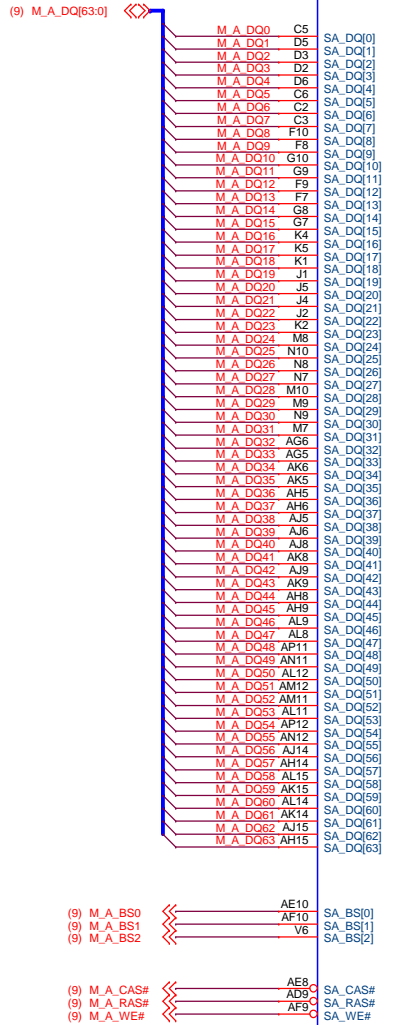
### eDP

Differential 85ohm (single 50)  
n,p mismatch <5mils  
pair to pair mismatch < 7 inches  
Max:  
4vias : 2000 - 5000 mils  
436735 Huron River Design Guide 1.0

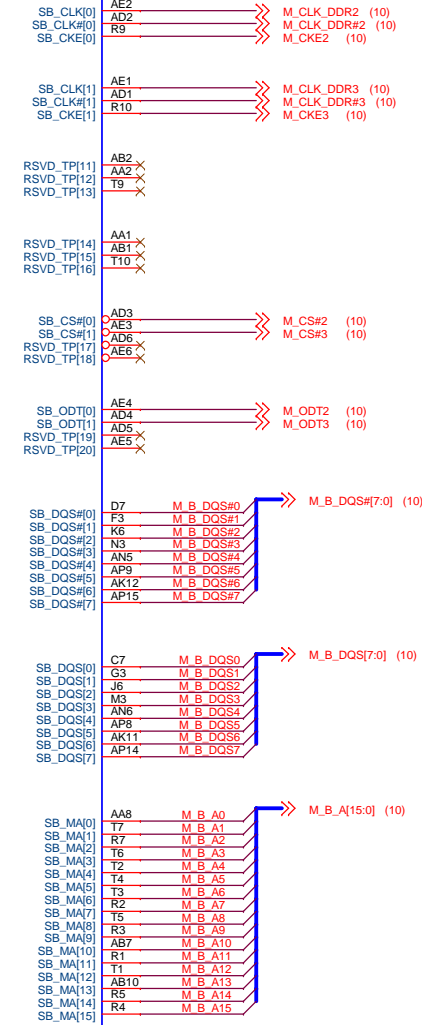




DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



Sandy Bridge\_FOXCNN\_PZ98927-3641-41F

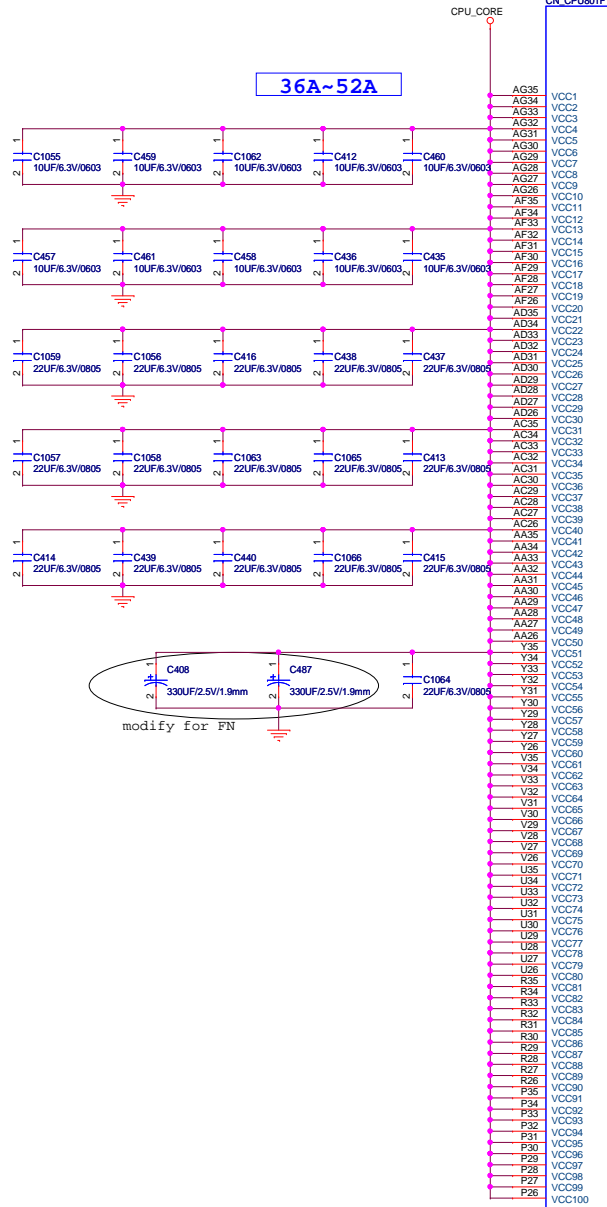
Sandy Bridge\_FOXCNN\_PZ98927-3641-41F

FLEX Computing

|                                 |  |                         |            |
|---------------------------------|--|-------------------------|------------|
| Project Name :<br>H710DI1       |  | Title :<br>CPU_3/7_DDR3 |            |
| Size :                          | Document Number :<br>HPMH-40GAB6600-B130 |                         | Rev :<br>B |
| Date: Monday, November 08, 2010 |  | Sheet : 4               | of 63      |



# POWER



PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

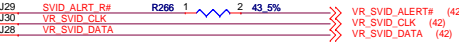
MB Bottom Socket Cavity

MB Top Socket Cavity

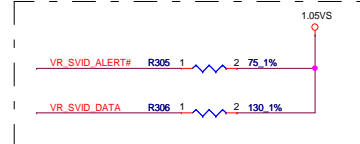
VCCIO at CPU

7/06 delet 330uF X2  
poewr side have 330uF X3  
(3x 330  $\mu$ F for 2012 capable designs)  
follow Huron River Platform Power Delivery (439028)

50 ohm reference GND

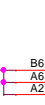
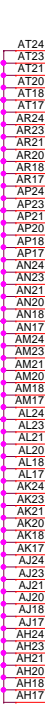


Layout Note:  
Alert#(AJ29) signal must be routed between  
the Clock and Data lines to reduce the cross  
talk between them. Spacing recommendations  
from the "Asynchronous Signal General  
Routing Guideline" of the Huron River  
PDG have to be met.





## GRAPHICS



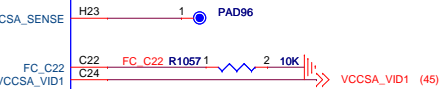
Sandy Bridge\_FOXCONN\_PZ98927-3641-41F

MISC

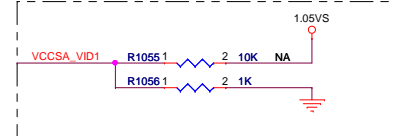
VCCSA\_SENS

FC\_C2

VCCSA\_VID



| VID[0]<br>Pin C22 | VID[1]<br>Pin C24 | VCCSA Vout | 2011<br>processor | 2012<br>processor |
|-------------------|-------------------|------------|-------------------|-------------------|
| 0                 | 0                 | 0.90 V     | Yes               | Yes               |
| 0                 | 1                 | 0.80 V     | Yes               | Yes               |
| 1                 | 0                 | 0.725 V    | No                | Yes               |
| 1                 | 1                 | 0.675 V    | No                | Yes               |



- EMI
- | Part | Value          |
|------|----------------|
| C450 | 0.1uF/16V/0402 |
| C456 | 0.1uF/16V/0402 |
| C468 | 0.1uF/16V/0402 |
| C472 | 0.1uF/16V/0402 |
- 4 pcs 0.1uF were recommend by Intel.  
But this purpose will be for EMI.  
JasonW 20100206

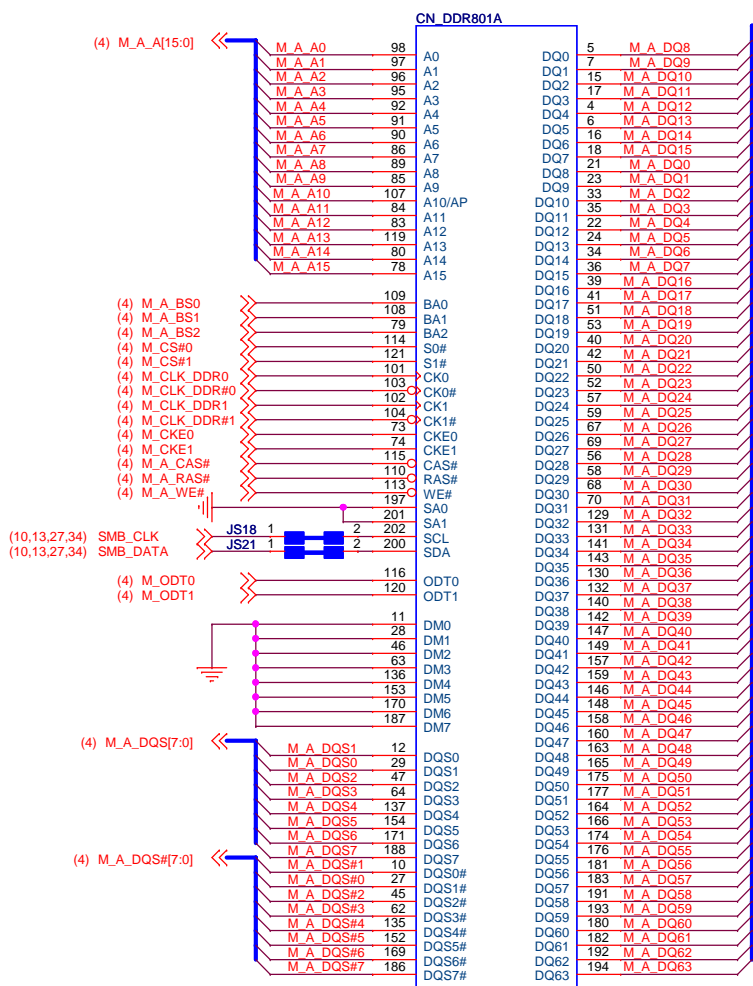
Four 0402 0.1uF stitching capacitors added  
between +V1.5\_DIMM & +V1.5S\_CPU\_VDDQ  
S3PowerReduction checklist

| VID[0]<br>Pin C22 | VID[1]<br>Pin C24 | VCCSA Vout | 2011<br>processor | 2012<br>processor |
|-------------------|-------------------|------------|-------------------|-------------------|
| 0                 | 0                 | 0.90 V     | Yes               | Yes               |
| 0                 | 1                 | 0.80 V     | Yes               | Yes               |
| 1                 | 0                 | 0.725 V    | No                | Yes               |
| 1                 | 1                 | 0.675 V    | No                | Yes               |



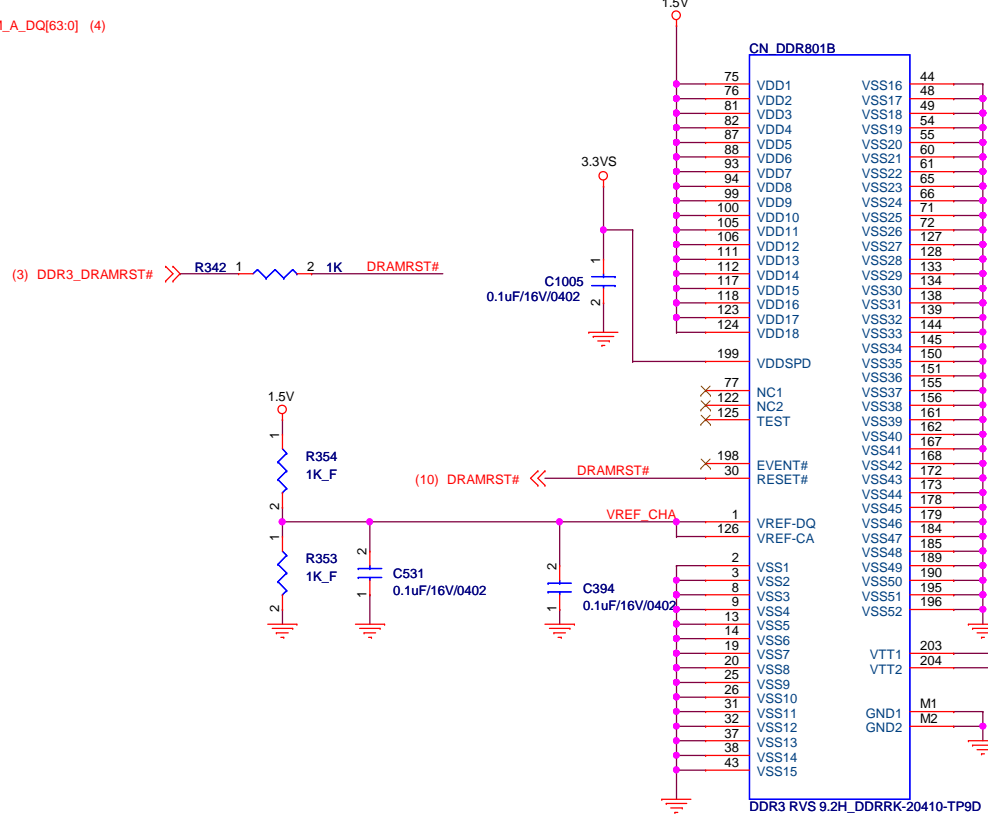


# Channel-A

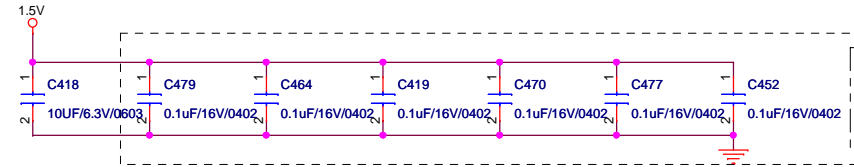


DDR3 RVS 9.2H\_DDRRK-20410-TP9D  
CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H

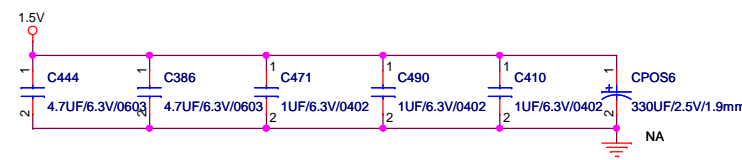
Note:  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30



CONN DDR3 RVS DDRRK-20410-TP9D 204P 9.2H



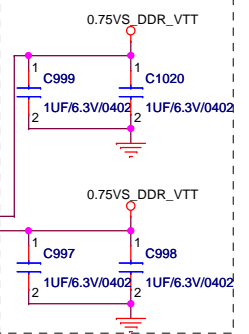
**Layout**  
0.1uF Caps for CMD,CLK,CTRL return path  
Place Caps on the same side as SO-DIMM  
and close to VDD Pin.



**FLEX**Computing

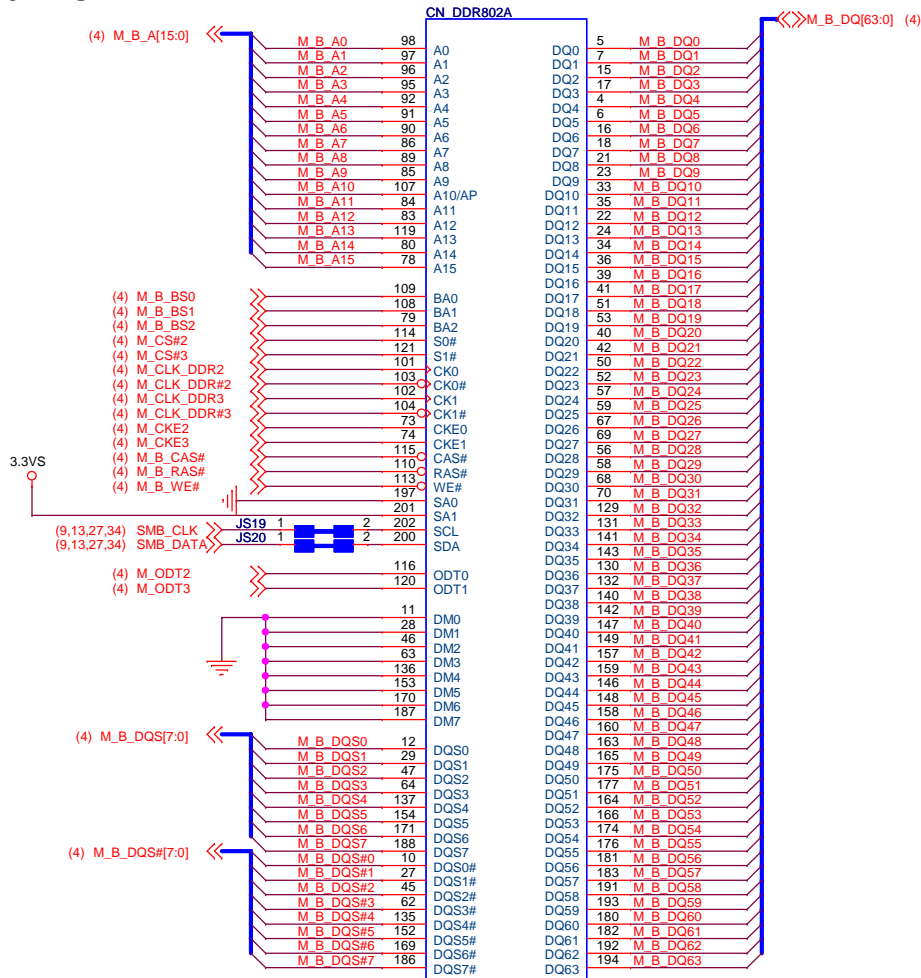
|                                  |                                       |                                |         |
|----------------------------------|---------------------------------------|--------------------------------|---------|
| Project Name : H710DI1           |                                       | Title : DDR3_SO-DIMM1 CHA(9H2) |         |
| Size :                           | Document Number : HPMH-40GAB6600-B130 |                                | Rev : B |
| Date : Monday, November 08, 2010 |                                       | Sheet : 9                      | of 63   |

**Layout**  
Place these caps close to Pin203 and 204.



Follow Intel CRB & CHKList 1uF x 4  
Due to Manchester SODIMM not butterfly,  
The decoupling ability can not share to 2 DIMMs.  
JasonW20100206

Channel-B

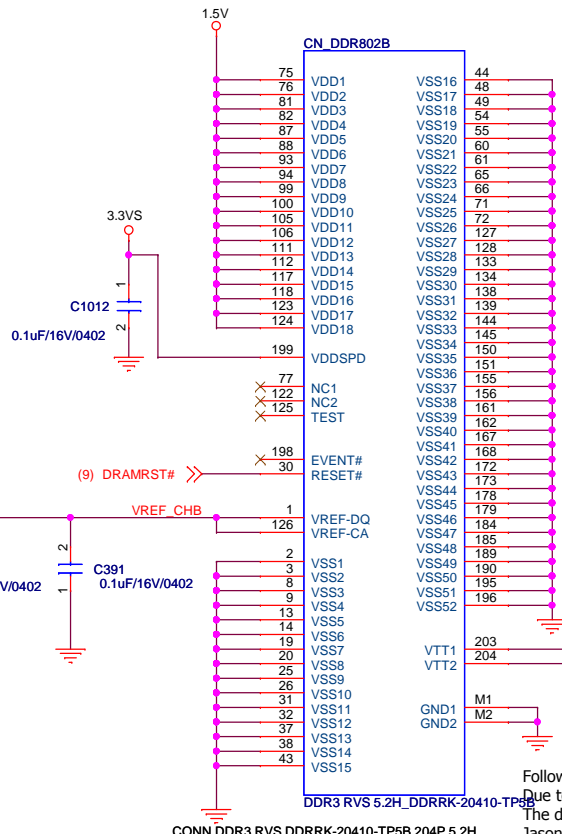


DDR3 RVS 5.2H\_DDRRK-20410-TP5B  
CONN DDR3 RVS DDRRK-20410-TP5B 204P 5.2H

| SO-DIMM Address            |     |      |  |
|----------------------------|-----|------|--|
| SA0_DIM0 = 0, SA1_DIM0 = 0 | SPD | 0xA0 |  |
|                            | TS  | 0x30 |  |
| SA0_DIM1 = 0, SA1_DIM1 = 1 | SPD | 0xA4 |  |
|                            | TS  | 0x34 |  |

Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

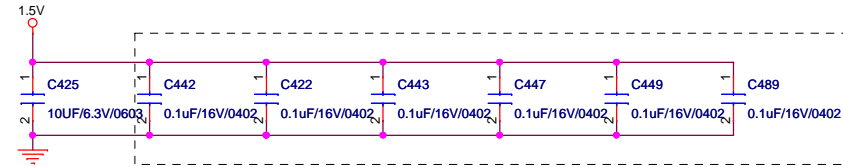
7/26 Matutina Modify



DDR3 RVS 5.2H\_DDRRK-20410-TP5B  
CONN DDR3 RVS DDRRK-20410-TP5B 204P 5.2H

**Layout**  
Place these caps close to Pin203 and 204.

Follow Intel CRB & CHKList 1uF x 4  
Due to Manchester SODIMM not butterfly,  
The decoupling ability can not share to 2 DIMMs.  
JasonW20100206

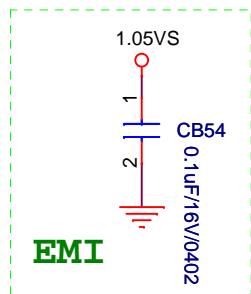
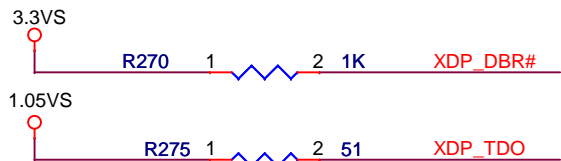
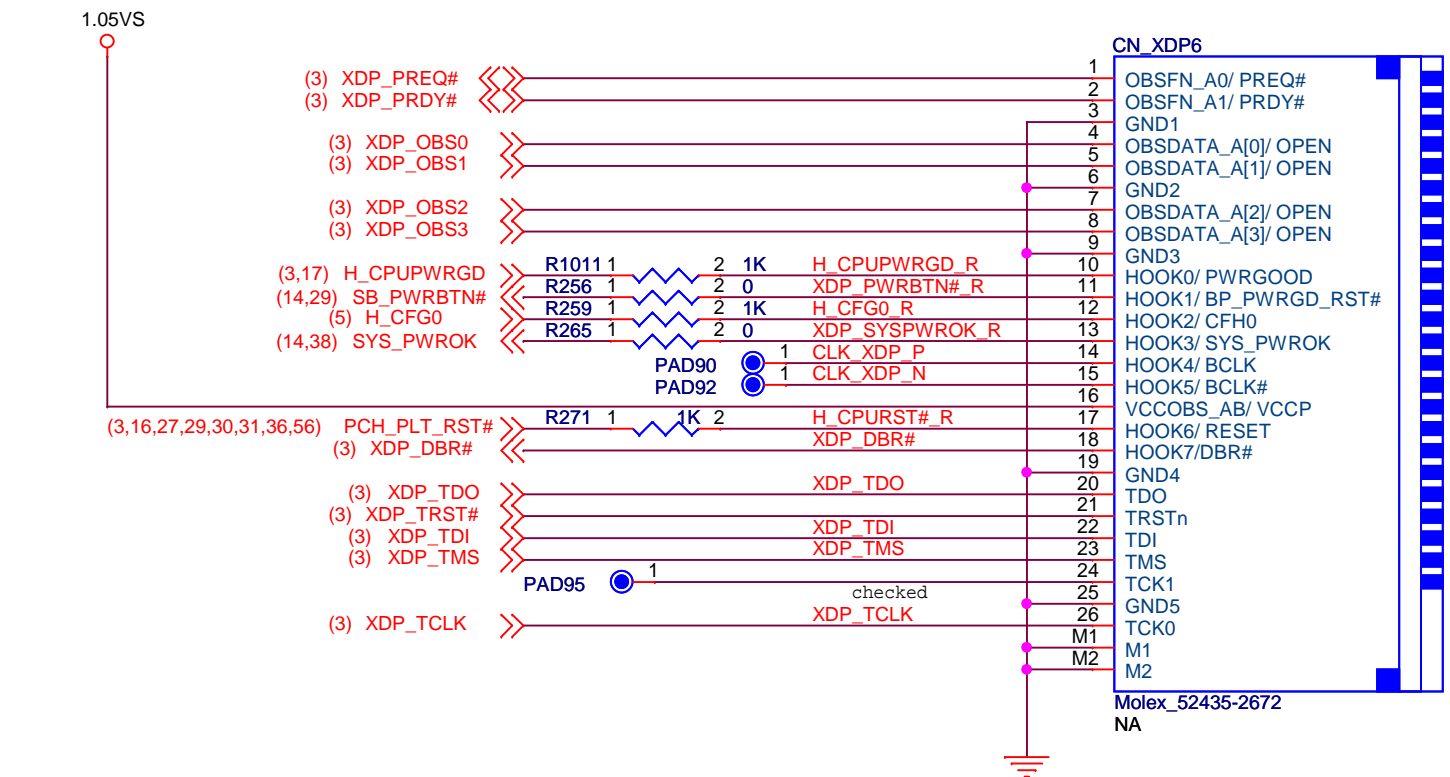


**Layout**  
0.1uF Caps for CMD,CLK,CTRL return path  
Place Caps on the same side as SO-DIMM  
and close to VDD Pin .

**FLEX**Computing

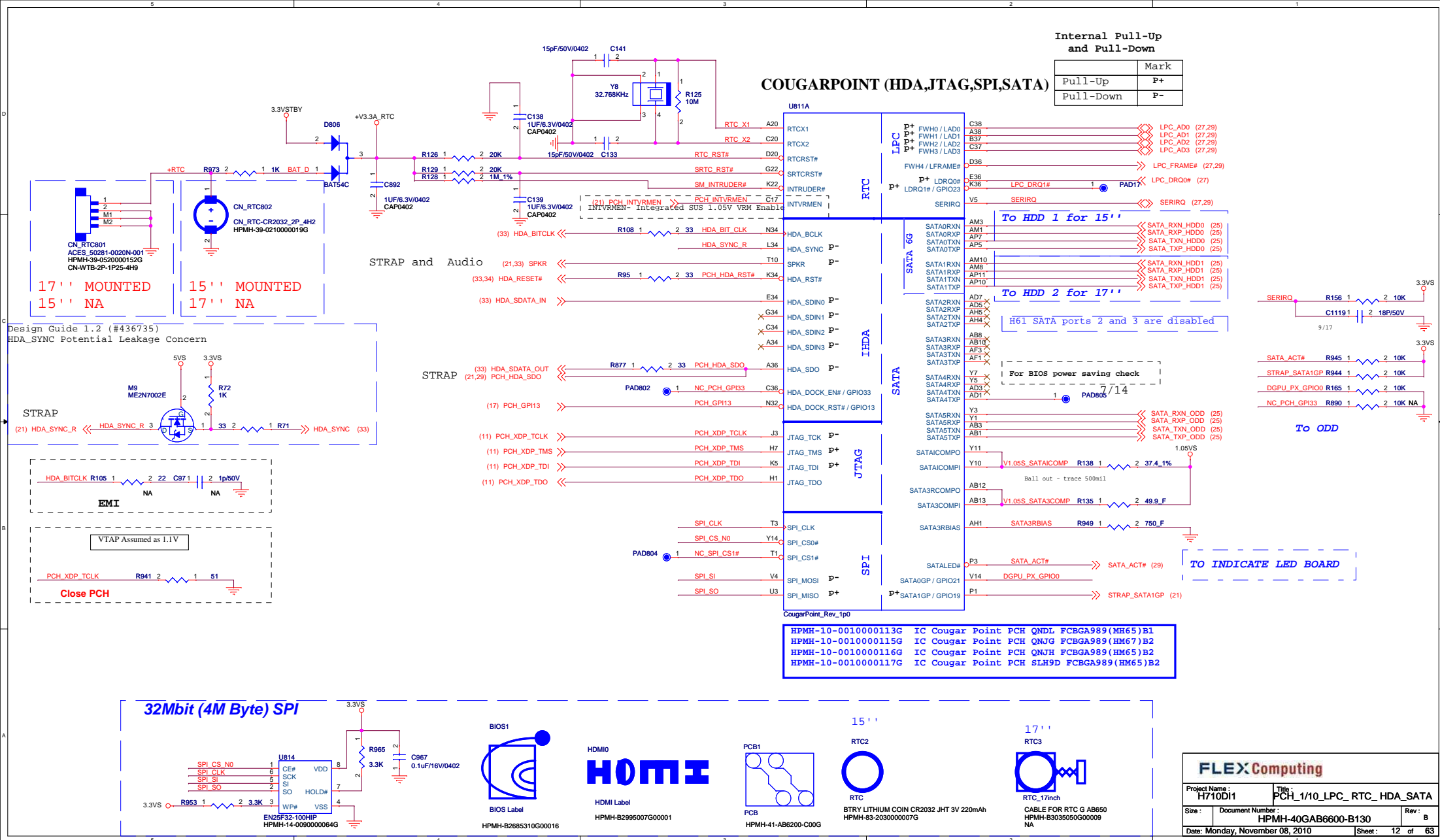
|                                  |                   |         |                        |
|----------------------------------|-------------------|---------|------------------------|
| Project Name :                   | H710DI1           | Title : | DDR3_SO-DIMM2 CHB(5H2) |
| Size :                           | Document Number : | Rev :   | B                      |
| HPMH-40GAB6600-B130              |                   |         |                        |
| Date : Monday, November 08, 2010 | Sheet :           | 10      | of 63                  |

# Debug Port



**FLEX** Computing

|                                 |  |                                 |            |
|---------------------------------|--|---------------------------------|------------|
| Project Name :<br>H710DI1       |  | Title :<br>XDP(PROCESSOR / PCH) |            |
| Size :                          | Document Number :<br>HPMH-40GAB6600-B130 |                                 | Rev :<br>B |
| Date: Monday, November 08, 2010 |  | Sheet :                         | 11 of 63   |





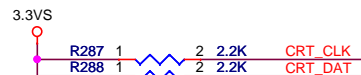
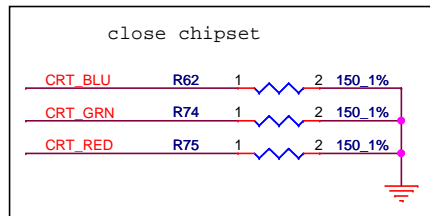
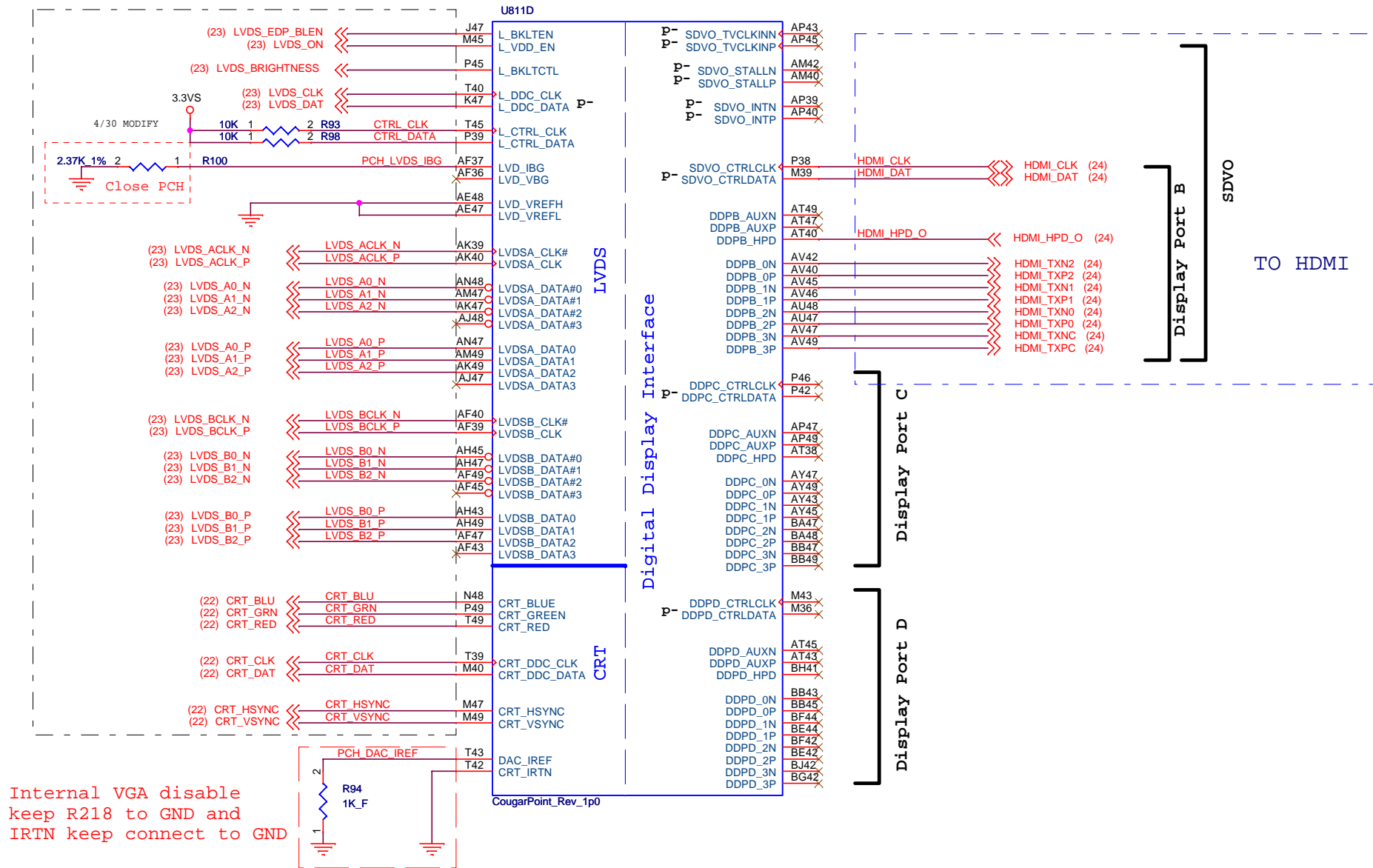


3.3VSTBY\_PCH

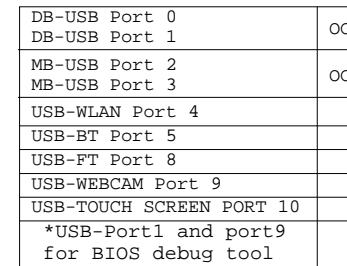




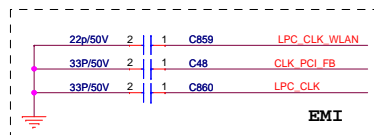
# COUGARPOINT (LVDS,DDI)



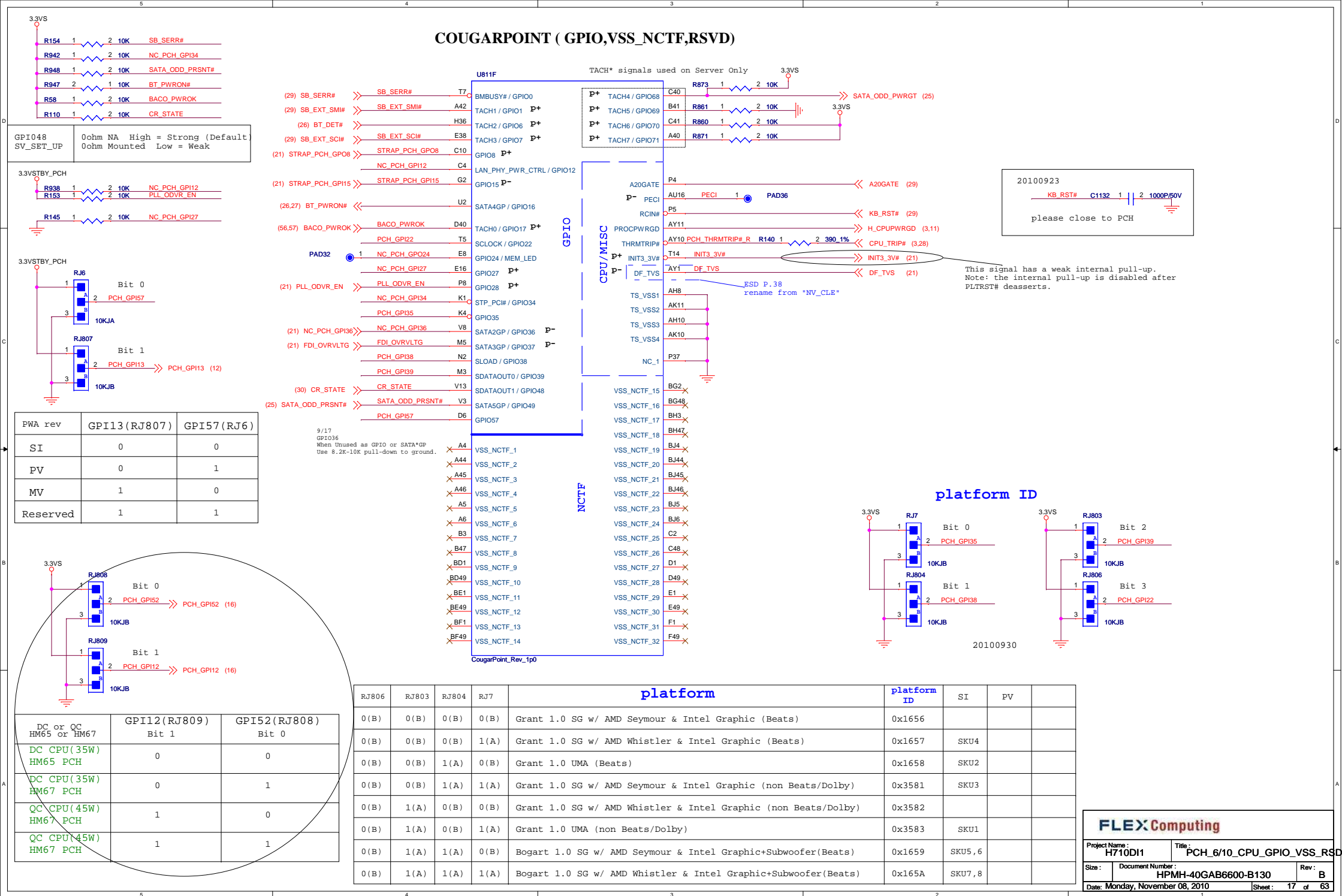
| U811E |  |  |        |      |
|-------|--|--|--------|------|
|       |  |  | RSVD1  | A7   |
|       |  |  | RSVD2  | A7   |
|       |  |  | RSVD3  | A8   |
|       |  |  | RSVD4  | B8   |
|       |  |  | RSVD5  | AT10 |
|       |  |  | RSVD6  | BC8  |
|       |  |  | RSVD7  | AU2  |
|       |  |  | RSVD8  | AT4  |
|       |  |  | RSVD9  | AT3  |
|       |  |  | RSVD10 | AT1  |
|       |  |  | RSVD11 | AY3  |
|       |  |  | RSVD12 | AT5  |
|       |  |  | RSVD13 | AV3  |
|       |  |  | RSVD14 | AV1  |
|       |  |  | RSVD15 | BB1  |
|       |  |  | RSVD16 | BA3  |
|       |  |  | RSVD17 | BB5  |
|       |  |  | RSVD18 | BB3  |
|       |  |  | RSVD19 | BB7  |
|       |  |  | RSVD20 | BB9  |
|       |  |  | RSVD21 | BD4  |
|       |  |  | RSVD22 | BF6  |
|       |  |  | RSVD23 | AV5  |
|       |  |  | RSVD24 | AV10 |
|       |  |  | RSVD25 | AT8  |
|       |  |  | RSVD26 | AY5  |
|       |  |  | RSVD27 | BA2  |
|       |  |  | RSVD28 | AT12 |
|       |  |  | RSVD29 | BF3  |



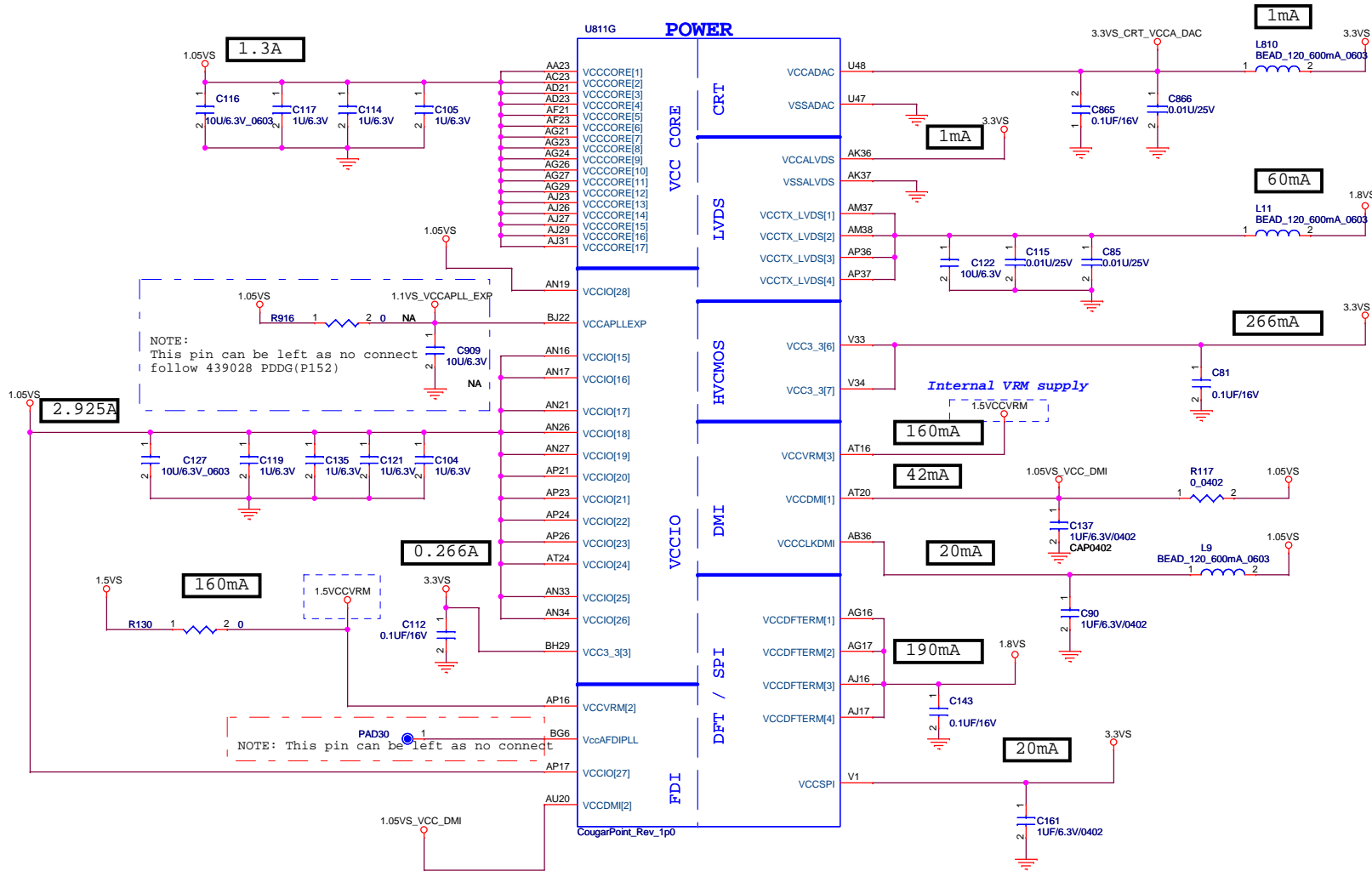
- 
- Timing diagram for USB signals. The diagram shows five signals: USB\_OC0#, USB\_OC1#, NC\_PCH\_USB\_OC2, NC\_PCH\_USB\_OC4, and WAKESCI#. Each signal is represented by a purple line with a resistor symbol and timing parameters. USB\_OC0# has R907, 1, 2, 10K. USB\_OC1# has R127, 1, 2, 10K. NC\_PCH\_USB\_OC2 has R901, 1, 2, 10K. NC\_PCH\_USB\_OC4 has R903, 1, 2, 10K. WAKESCI# has R905, 2, 1, 10K. A 3.3VSTBY\_PCH signal is shown at the top right.



# COUGARPOINT ( GPIO,VSS\_NCTF,RSVD)

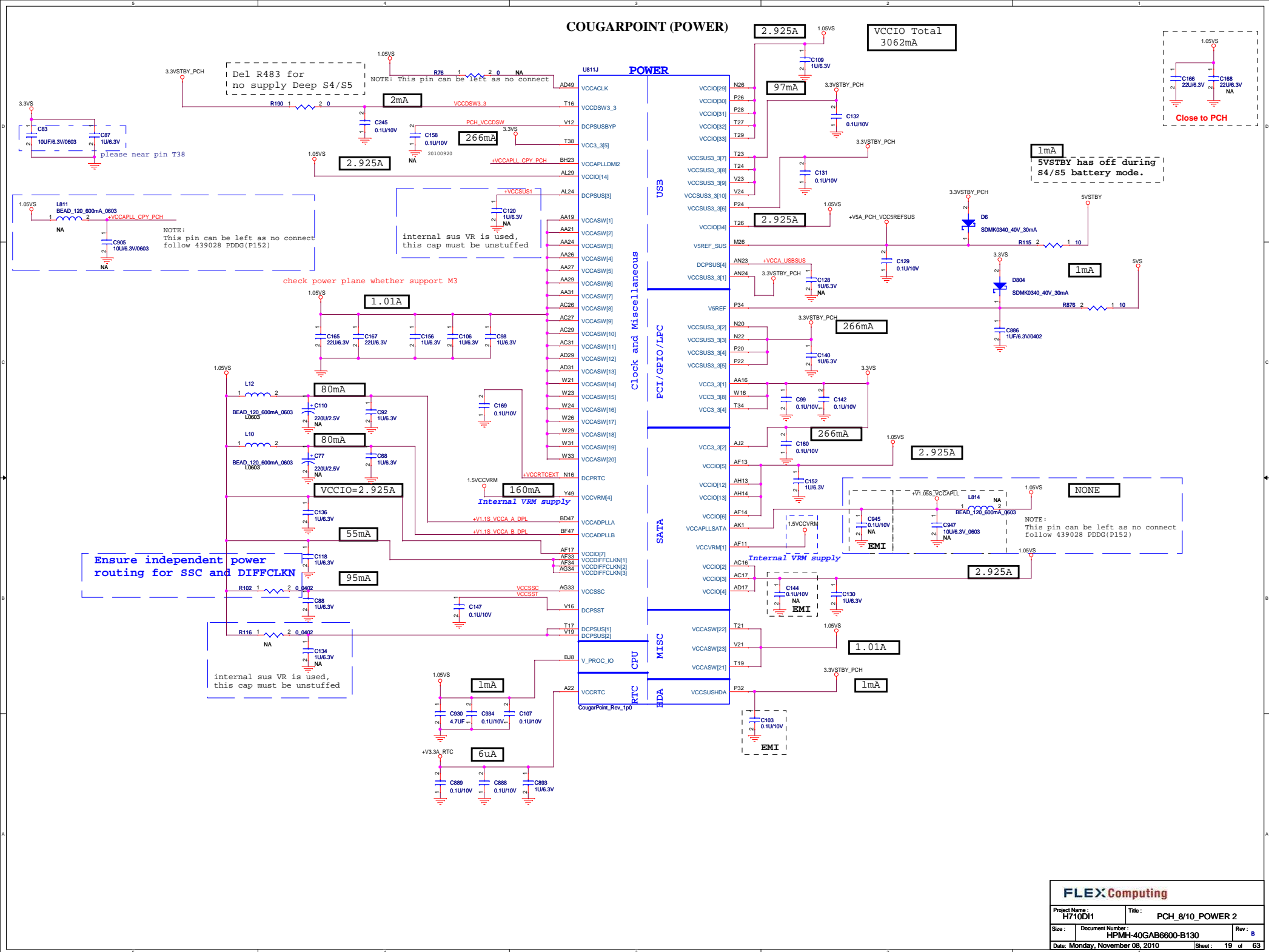


# COUGARPOINT (POWER)



|                                 |                     |          |
|---------------------------------|---------------------|----------|
| <b>FLEX Computing</b>           |                     |          |
| Project Name :                  | H710D11             |          |
| Title :                         | PCH_7/10_POWER 1    |          |
| Size :                          | Document Number :   | Rev :    |
|                                 | HPMH-40GAB6600-B130 | B        |
| Date: Monday, November 08, 2010 | Sheet :             | 18 of 63 |

### COUGARPOINT (POWER)



COUGARPOINT (GND)

U811I

|      |          |      |
|------|----------|------|
| AY4  | VSS[159] | H46  |
| AY42 | VSS[160] | K18  |
| AY46 | VSS[161] | K26  |
| AY8  | VSS[162] | K39  |
| B11  | VSS[163] | K46  |
| B15  | VSS[164] | K7   |
| B19  | VSS[165] | L18  |
| B23  | VSS[166] | L2   |
| B27  | VSS[167] | L20  |
| B31  | VSS[168] | L26  |
| B35  | VSS[169] | L28  |
| B39  | VSS[170] | L36  |
| B7   | VSS[171] | L46  |
| F45  | VSS[172] | M12  |
| BB12 | VSS[173] | M18  |
| BB16 | VSS[174] | M22  |
| BB20 | VSS[175] | M24  |
| BB22 | VSS[176] | M30  |
| BB24 | VSS[177] | M32  |
| BB28 | VSS[178] | M34  |
| BB30 | VSS[179] | M38  |
| BB38 | VSS[180] | M4   |
| BB4  | VSS[181] | M42  |
| BB46 | VSS[182] | M46  |
| BC14 | VSS[183] | M8   |
| BC18 | VSS[184] | N18  |
| BC2  | VSS[185] | P30  |
| BC22 | VSS[186] | N47  |
| BC26 | VSS[187] | P11  |
| BC32 | VSS[188] | P18  |
| BC34 | VSS[189] | T33  |
| BC36 | VSS[190] | P40  |
| BC40 | VSS[191] | P43  |
| BC42 | VSS[192] | P47  |
| BC48 | VSS[193] | P7   |
| BD46 | VSS[194] | R2   |
| BD5  | VSS[195] | R48  |
| BE22 | VSS[196] | T12  |
| BE26 | VSS[197] | T37  |
| BE40 | VSS[198] | T4   |
| BF10 | VSS[199] | W34  |
| BF12 | VSS[200] | T46  |
| BF16 | VSS[201] | T47  |
| BF20 | VSS[202] | T8   |
| BF22 | VSS[203] | V11  |
| BF24 | VSS[204] | V17  |
| BF26 | VSS[205] | V26  |
| BF28 | VSS[206] | V27  |
| BD3  | VSS[207] | V29  |
| BF30 | VSS[208] | V31  |
| BF38 | VSS[209] | V36  |
| BF40 | VSS[210] | V39  |
| BF8  | VSS[211] | V43  |
| BG17 | VSS[212] | V7   |
| BG21 | VSS[213] | W17  |
| BG33 | VSS[214] | W19  |
| BG44 | VSS[215] | W2   |
| BG8  | VSS[216] | W27  |
| BH11 | VSS[217] | W48  |
| BH15 | VSS[218] | Y12  |
| BH17 | VSS[219] | Y38  |
| BH19 | VSS[220] | Y4   |
| H10  | VSS[221] | Y42  |
| BH27 | VSS[222] | Y46  |
| BH31 | VSS[223] | Y8   |
| BH33 | VSS[224] | BG29 |
| BH35 | VSS[225] | N24  |
| BH39 | VSS[226] | AJ3  |
| BH43 | VSS[227] | AD47 |
| BH7  | VSS[228] | B43  |
| D3   | VSS[229] | BE10 |
| D12  | VSS[230] | BG41 |
| D16  | VSS[231] | G14  |
| D18  | VSS[232] | H16  |
| D22  | VSS[233] | T36  |
| D24  | VSS[234] | BG22 |
| D26  | VSS[235] | AJ34 |
| D30  | VSS[236] | AJ33 |
| D32  | VSS[237] | C22  |
| D34  | VSS[238] | AK12 |
| D38  | VSS[239] | AK3  |
| D42  | VSS[240] | AP13 |
| D8   | VSS[241] | M14  |
| E18  | VSS[242] | AP3  |
| E26  | VSS[243] | AP1  |
| G18  | VSS[244] | BE16 |
| G20  | VSS[245] | BC16 |
| G26  | VSS[246] | BG28 |
| G28  | VSS[247] | BJ28 |
| G36  | VSS[248] |      |
| G48  | VSS[249] |      |
| H12  | VSS[250] |      |
| H18  | VSS[251] |      |
| H22  | VSS[252] |      |
| H24  | VSS[253] |      |
| H26  | VSS[254] |      |
| H30  | VSS[255] |      |
| H32  | VSS[256] |      |
| H34  | VSS[257] |      |
| F3   | VSS[258] |      |

CougarPoint\_Rev\_1p0

U811H

|      |         |      |
|------|---------|------|
| H5   | VSS[0]  | AK38 |
| AA17 | VSS[1]  | AK4  |
| AA2  | VSS[2]  | AK42 |
| AA3  | VSS[3]  | AK46 |
| AA33 | VSS[4]  | AK8  |
| AA34 | VSS[5]  | AL16 |
| AB11 | VSS[6]  | AL17 |
| AB14 | VSS[7]  | AL19 |
| AB39 | VSS[8]  | AL2  |
| AB4  | VSS[9]  | AL21 |
| AB43 | VSS[10] | AL23 |
| AB5  | VSS[11] | AL26 |
| AB7  | VSS[12] | AL27 |
| AC19 | VSS[13] | AL31 |
| AC2  | VSS[14] | AL33 |
| AC21 | VSS[15] | AL34 |
| AC24 | VSS[16] | AL48 |
| AC33 | VSS[17] | AM11 |
| AC34 | VSS[18] | AM14 |
| AC48 | VSS[19] | AM36 |
| AD10 | VSS[20] | AM39 |
| AD11 | VSS[21] | AM43 |
| AD12 | VSS[22] | AM45 |
| AD13 | VSS[23] | AM46 |
| AD19 | VSS[24] | AM7  |
| AD24 | VSS[25] | AN2  |
| AD26 | VSS[26] | AN29 |
| AD27 | VSS[27] | AN3  |
| AD33 | VSS[28] | AN31 |
| AD34 | VSS[29] | AP12 |
| AD36 | VSS[30] | AP19 |
| AD37 | VSS[31] | AP28 |
| AD38 | VSS[32] | AP30 |
| AD39 | VSS[33] | AP32 |
| AD4  | VSS[34] | AP38 |
| AD40 | VSS[35] | AP4  |
| AD42 | VSS[36] | AP42 |
| AD43 | VSS[37] | AP46 |
| AD45 | VSS[38] | AP8  |
| AD46 | VSS[39] | AR2  |
| AD8  | VSS[40] | AR48 |
| AE2  | VSS[41] | AT11 |
| AE3  | VSS[42] | AT13 |
| AF10 | VSS[43] | AT18 |
| AF12 | VSS[44] | AT22 |
| AD14 | VSS[45] | AT26 |
| AF16 | VSS[46] | AT28 |
| AF19 | VSS[47] | AT30 |
| AF24 | VSS[48] | AT32 |
| AF26 | VSS[49] | AT34 |
| AF27 | VSS[50] | AT38 |
| AF29 | VSS[51] | AT42 |
| AF31 | VSS[52] | AT46 |
| AF38 | VSS[53] | AT7  |
| AF4  | VSS[54] | AU24 |
| AF42 | VSS[55] | AU30 |
| AF46 | VSS[56] | AV16 |
| AF5  | VSS[57] | AV20 |
| AF7  | VSS[58] | AV24 |
| AF8  | VSS[59] | AV30 |
| AG19 | VSS[60] | AV38 |
| AG2  | VSS[61] | AV4  |
| AG27 | VSS[62] | AV43 |
| AG31 | VSS[63] | AV8  |
| AG48 | VSS[64] | AW14 |
| AH11 | VSS[65] | AW18 |
| AH3  | VSS[66] | AW2  |
| AH36 | VSS[67] | AW22 |
| AH39 | VSS[68] | AW26 |
| AH40 | VSS[69] | AW28 |
| AH42 | VSS[70] | AW32 |
| AH46 | VSS[71] | AW34 |
| AH7  | VSS[72] | AW36 |
| AJ19 | VSS[73] | AW40 |
| AJ21 | VSS[74] | AW48 |
| AJ24 | VSS[75] | AV11 |
| AJ33 | VSS[76] | AV12 |
| AJ34 | VSS[77] | AV22 |
| AK12 | VSS[78] | AY28 |
| AK3  | VSS[79] |      |

CougarPoint\_Rev\_1p0

FLEX Computing

Project Name :  
H710D11

Title :  
PCH\_9/10\_GND

Size :

Document Number :  
HPMH-40GAB6600-B130

Rev :  
B

Date: Monday, November 08, 2010

Sheet: 20 of 63



| Signal           | Usage   | When Sampled               | Internal PULL  | Comment  |
|------------------|---|----------------------------|--|--|
| SPKR             | No Reboot   | Rising edge of PWROK       | Internal PD<br>(The internal PD is disabled after PLTRST# de-asserts)          | H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode<br>L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers' Offset (3410h:Bit 5)).<br><b>Default</b> |
| INIT3_3V#        | Reserved  | Rising edge of PWROK       | Internal PU<br>(The internal PU is disabled after PLTRST# de-asserts)          | This signal should not be pulled low   |
| GNT[3]#/GPIO[55] | Top-Block Swap Override                           | Rising edge of PWROK       | Internal PU<br>(The internal PU is disabled after PLTRST# de-asserts)          | H: Top Block Swap Mode disabled<br><b>Default</b><br>L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode  |
| INTVRMEN         | Integrated 1.05 V VRM Enable / Disable            | Always                     | NA   | H: Integrated 1.05V VRMs enabled<br><b>Default</b><br>This signal should always be External pulled high<br>L: Integrated 1.05V VRMs disabled   |
| GNT1#/GPIO51/    | Boot BIOS Strap bit [1] BBS[1]                    | Rising edge of PWROK       | Internal PU<br>(The internal PU is disabled after PLTRST# de-asserts)          | GNT1# SATA1GP Boot BIOS Location<br>0 0 LPC<br>0 1 Reserved<br>1 0 PCI<br>1 1 SPI<br><b>Default</b>  |
| SATA1GP/ GPIO19  | Boot BIOS Strap bit[0] BBS[0]                     | Rising edge of PWROK       | Internal PU<br>(The internal PU is disabled after PLTRST# de-asserts)          |  |
| GNT2#/GPIO53     | ESI Strap (Server Only)                           | Rising edge of PWROK       | Internal PU<br>(The internal PU is disabled after PLTRST# de-asserts)          | H: Should not be pulled low for desktop and mobile<br><b>Default</b><br>ESI compatible mode is for server platforms only.<br>L: Configures DMI for ESI compatible operation  |
| HDA_SDO          | Flash Descriptor Security Override/ ME Debug Mode | Rising edge of RSMRST#     | Internal PD  | H: If sampled high,the Flash Descriptor Security will be overridden.<br>L: If strap is sampled low, ( Default ) the security measures defined in the Flash Descriptor will be in effect.<br>This signal should not be pulled high          |
| DF_TVS           | DMI and FDI Tx/ Rx Termination Voltage            | Rising edge of PWROK       | Internal PD  | The internal pull-down is disabled after PLTRST# deasserts   |
| GPIO28           | On-Die PLL Voltage Regulator                      | Rising edge of RSMRST# pin | Internal PU  | H: The On-Die PLL voltage regulator is enabled when sampled high<br><b>Default</b><br>L: When sampled low the On-Die PLL Voltage Regulator is disabled   |
| HDA_SYNC         | On-Die PLL Voltage Regulator Voltage Select       | Rising edge of RSMRST# pin | Internal PD  | H: On-Die PLL VR is supplied by 1.5 V<br><b>Default</b><br>L: On-Die PLL VR is supplied by 1.8 V   |
| GPIO15           | TLS Confidentiality                               | Rising edge of RSMRST# pin | Internal PD<br>The weak internal pull-down is disabled after RSMRST# deasserts | H: Intel ME Crypto TLS cipher suite with confidentiality<br><b>Default</b><br>L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality   |
| L_DDC_DATA       | LVDS Detected                                     | Rising edge of PWROK       | Internal PD<br>The internal pull-down is disabled after PLTRST# deasserts.     | H:LVDS is detected<br><b>Default</b><br>L:LVDS is not detected   |
| SDVO_CTLRLDATA   | Port B Detected                                   | Rising Edge of PWROK       | Internal PD<br>(The internal PD is disabled after PLTRST# de-asserts)          | H:Port B is detected<br>L:Port B is not detected<br><b>Default</b>   |
| DDPC_CTLRLDATA   | Port C Detected                                   | Rising edge of PWROK       | Internal PD<br>(The internal PD is disabled after PLTRST# de-asserts)          | H: Port C is detected<br>L: Port C is not detected<br><b>Default</b>   |
| DDPD_CTLRLDATA   | Port D Detected                                   | Rising edge of PWROK       | Internal PD<br>(The internal PD is disabled after PLTRST# de-asserts)          | H: Port D is detected<br>L: Port D is not detected<br><b>Default</b>   |
| DSWVRMEN         | Deep S4/S5 Well On-Die Voltage Regulator Enable   | Always                     | NA   | If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.  |
| SATA2GP/ GPIO36  | Reserved  | Rising edge of PWROK       | Internal PD<br>(The internal pull-down is disabled after PLTRST# deasserts.)   | NOTE: This signal should not be pulled high when strap is sampled.   |
| SATA3GP/ GPIO37  | Reserved  | Rising edge of PWROK       | Internal PD<br>(The internal pull-down is disabled after PLTRST# deasserts.)   | NOTE:<br>NOTE: This signal should not be pulled high when strap is sampled.  |
| GPIO8            | Reserved  | Rising edge of RSMRST#     | Internal PU<br>(Pull-up is disabled after RSMRST# is deasserted.)              | NOTE: This signal should not be pulled low   |

PAD24 1 SPKR (12,33)

PAD21 1 INIT3\_3V# (17)

R70 1 2 1K NA STRAP\_GNT3# (16)

+V3.3A\_RTC  
R896 1 2 330K PCH\_INTVRMEN (12)

R69 1K NA R943 1K NA  
STRAP\_GNT1# (16)  
STRAP\_SATA1GP (12)

PAD10 1 STRAP\_GNT2# (16)

3.3VS  
R1115 1 2 1K NA PCH\_HDA\_SDO (12,29)

1.8VS  
R933 1 2 2.2K  
PLACE 2.2K CLOSE TO THE BRANCHING POINT  
(3) H\_SNB\_IVB# R929 1 2 1K DF\_TVS (17)

PAD35 1 PLL\_ODVR\_EN (17)

3.3VSTBY\_PCH  
R107 1 2 1K HDA\_SYNC\_R (12)

3.3VSTBY\_PCH  
R939 1 2 1K NA STRAP\_PCH\_GPI15 (17)

+V3.3A\_RTC  
R1067 1 2 330K  
R899 1 2 330K NA DSWODVREN (14)  
DSWODVREN

R1110 1 2 10K NC\_PCH\_GPI36 (17)

R181 1 2 10K FDI\_OVRVLTG (17)  
FDI\_OVRVLTG

R918 1 2 1K STRAP\_PCH\_GPO8 (17)

| NO REBOOT |                      |
|-----------|----------------------|
| NA        | Low=Disable(Default) |
| MOUNTED   | High=Enable          |

| A16 swap override Strap |   |
|-------------------------|---|
| STP_A160VR              | Low = A16 swap override<br>High = Default |

|  |
|--|
| INTVRMEN- Integrated SUS<br>1.05V VRM Enable |
|--|

| Flash Descriptor Security Override |  |
|------------------------------------|--|
| PCH_HDA_SDO                        | NA Low=Disable(Default)<br>MOUNTED High=Enable |

| DMI & FDI Termination Voltage |   |
|-------------------------------|---|
| DF_TVS                        | Set to Vss when LOW<br>Set to Vcc when HIGH |

| PLL ON DIE VR ENABLE |                                  |
|----------------------|----------------------------------|
| PLL_ODVR_EN          | ENABLE- UNSTUFF<br>DISABLE-STUFF |

HR only support 1.5 V  
HDA\_SYNC need PU to HDA SUS rail through 1k ohm  
for 451710\_451710 SPEC

| DSWODVREN - On Die DSW VR Enable |                  |
|----------------------------------|------------------|
| Pull High                        | Enable (Default) |
| Pull Down                        | Disable          |

| DMI TERMINATION VOLTAGE OVERRIDE |  |
|----------------------------------|--|
| GPIO36                           | LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT |

| FDI TERMINATION VOLTAGE OVERRIDE |  |
|----------------------------------|--|
| GPIO37 (FDI_OVRVLTG)             | LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT |

|   |
|---|
| GPIO8 Integrated Clock Chip Enable      |
| High : Disable<br>Low : Enable(default) |

| FLEXComputing                   |                                       |                         |   |
|---------------------------------|---------------------------------------|-------------------------|---|
| Project Name : H710DI1          |                                       | Title : PCH_10/10_STRAP |   |
| Size :                          | Document Number : HPMH-40GAB6600-B130 | Rev :                   | B |
| Date: Monday, November 08, 2010 |                                       | Sheet: 21 of 63         |   |

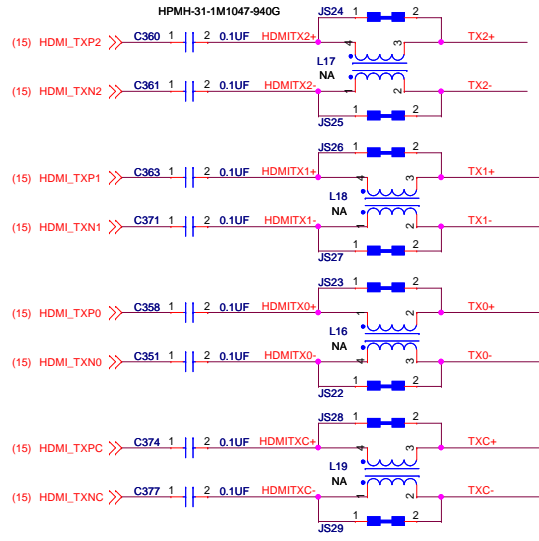




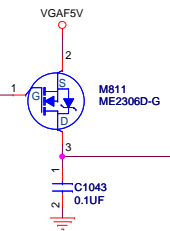
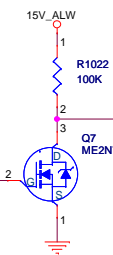
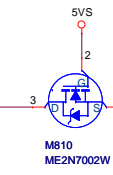
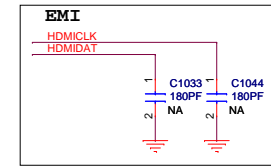
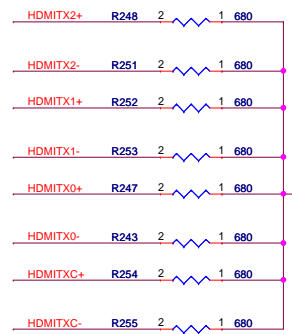
# HDMI

CLOSE to CN\_HDMI1

HPMH-32-4000000104G

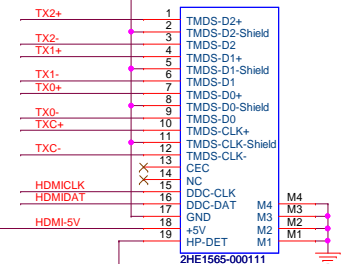


Intel Huron River: 680 ohm  
AMD Danube: 715 ohm  
AMD Sabine: 715 ohm

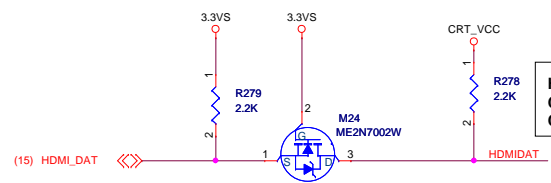


# HDMI

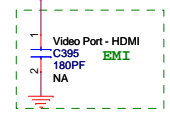
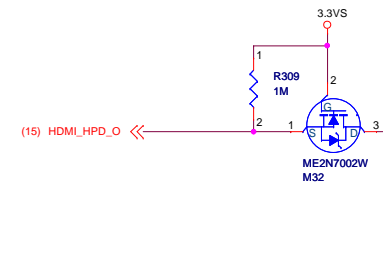
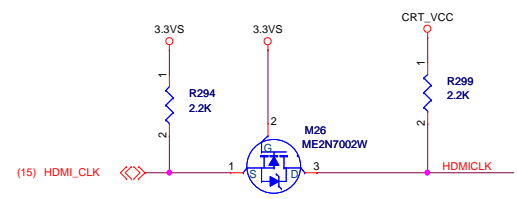
CN\_HDMI801



2HE1565-000111  
CN-HDMI-19DIP-7H1-RVS  
HPMH-38-00F0000017G



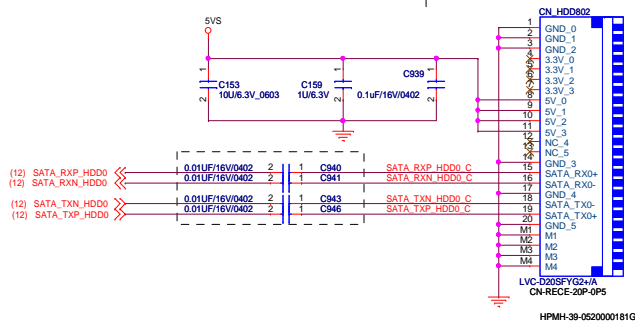
HDMI test  
C1 -- Cp=45pf  
C2 -- Cp=46pf (spec<50pf)



| FLEX Computing                   |                                       |                   |         |
|----------------------------------|---------------------------------------|-------------------|---------|
| Project Name : H710DI1           |                                       | Title : HDMI CONN |         |
| Size : Custom                    | Document Number : HPMH-40GAB6600-B130 |                   | Rev : B |
| Date : Monday, November 08, 2010 |                                       | Sheet : 24        | of 63   |

## HDD

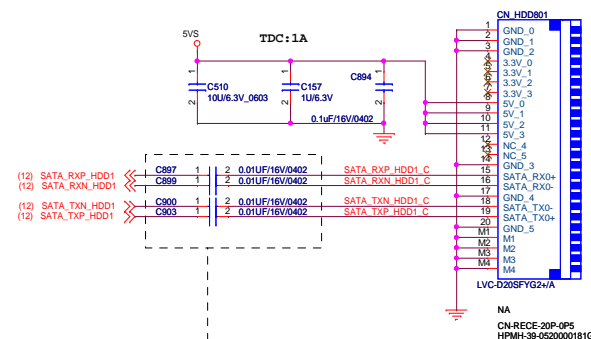
**Layout Notice:**  
0.01uF series cap close to connector  
follow SATA Signal Connection Checklist



## 2nd HDD

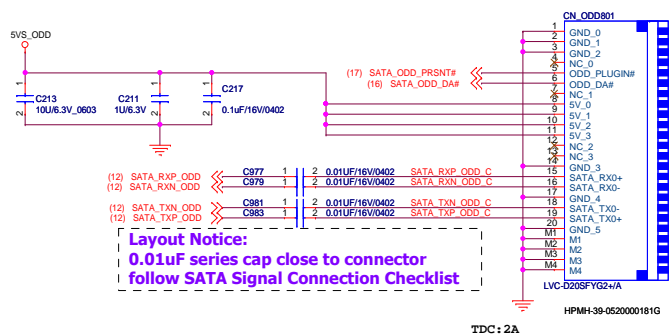
FOR 17" MB USE WTB CONNECTOR

CONN SPEC: 0.3A/PIN



**Layout Notice:**  
0.01uF series cap close to connector  
follow SATA Signal Connection Checklist

## ODD



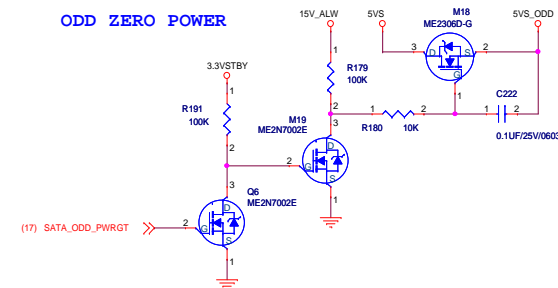
**Layout Notice:**  
0.01uF series cap close to connector  
follow SATA Signal Connection Checklist

TDC: 2A

Change to Cable type Conn

## ODD Zero Power

Check if meet max current!!



## G-Sensor

## G-SENSOR

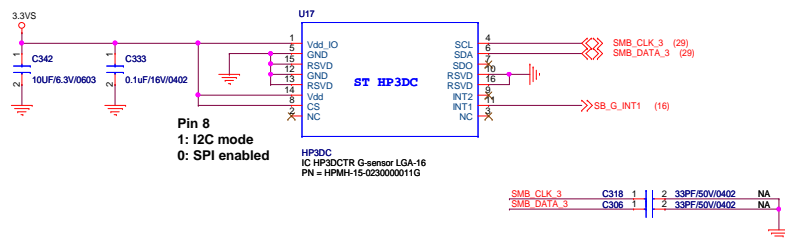
ST HP3DC

3.3VS

ADDR: 0011000x(30h) - SDO PD

ADDR: 0011010x(32h) - SDO NC

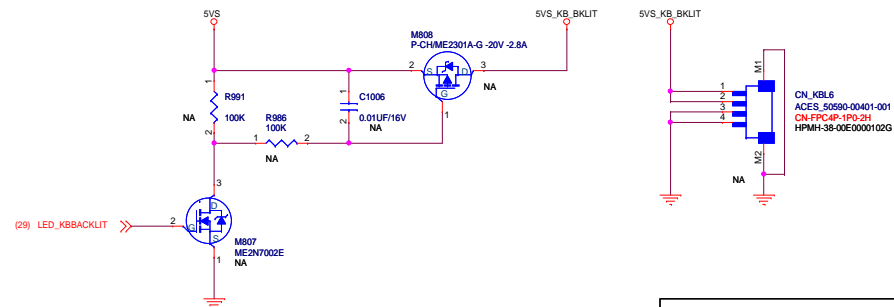
SINK: ??mA@VoL=0.33V(MAX)



Pin 8  
1: I2C mode  
0: SPI enabled

HP3DC  
IC HP3DCTR G-sensor LGA-16  
PN = HPMH-15-023000011G

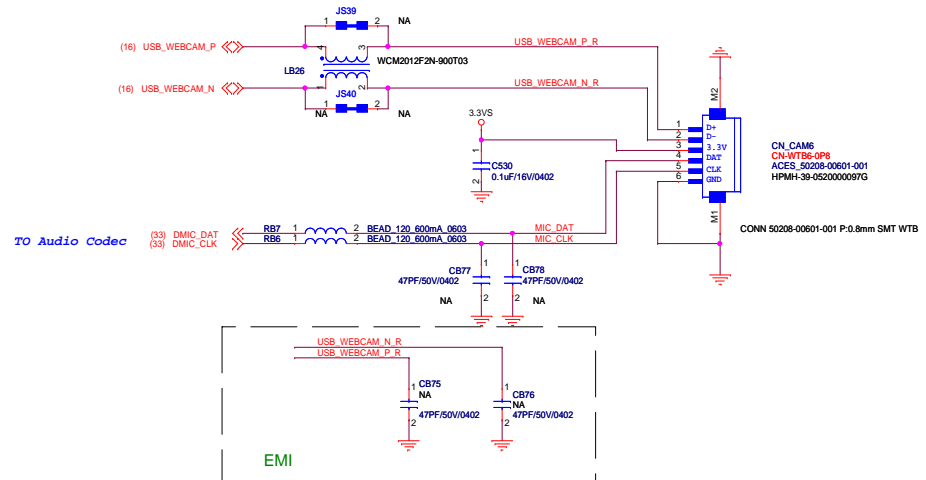
## KB Backlit



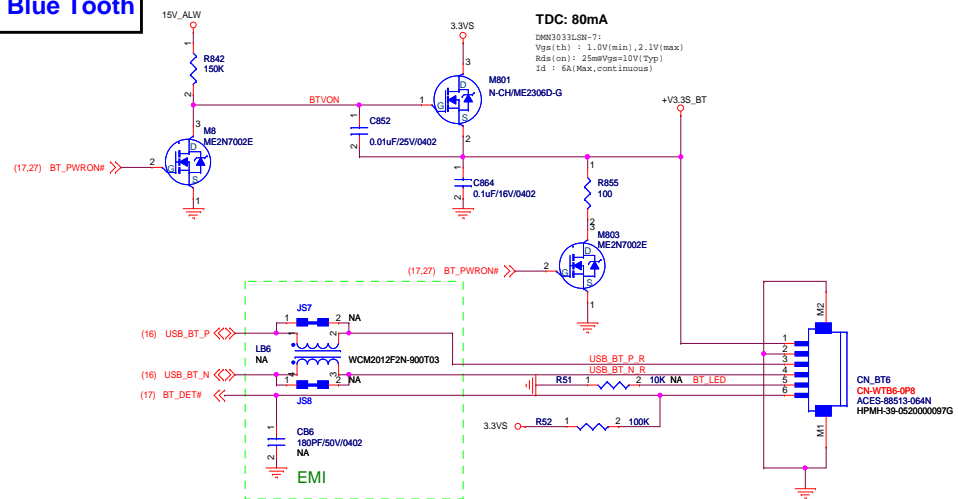
FLEX Computing

|               |                           |                     |                         |
|---------------|---------------------------|---------------------|-------------------------|
| Project Name: | H710D11                   | Title:              | HDD_ODD_G-Sensor_KB BKL |
| Size:         | Document Number:          | HPMH-40GAB6600-B130 | Rev: B                  |
| Date:         | Monday, November 08, 2010 | Sheet:              | 25 of 63                |

## Web CAM



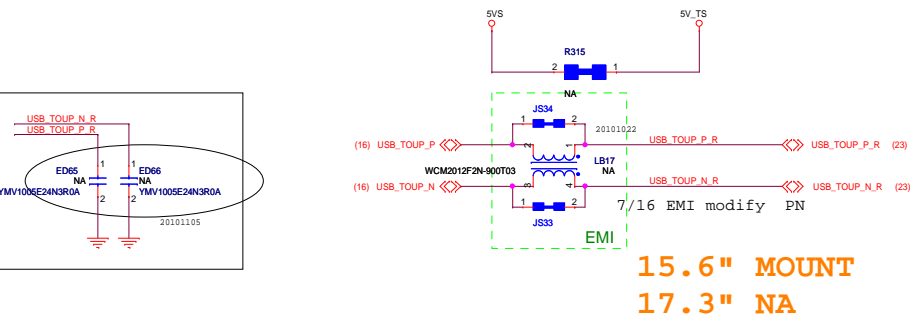
## Blue Tooth



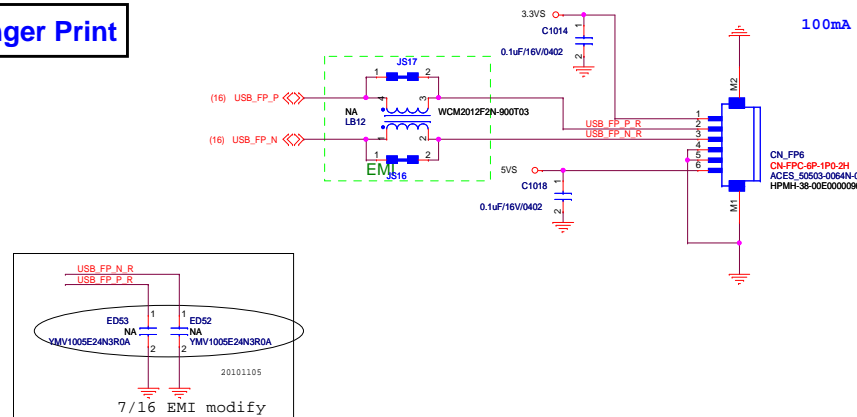
## TouchScreen

Touch Screen power is 5V type

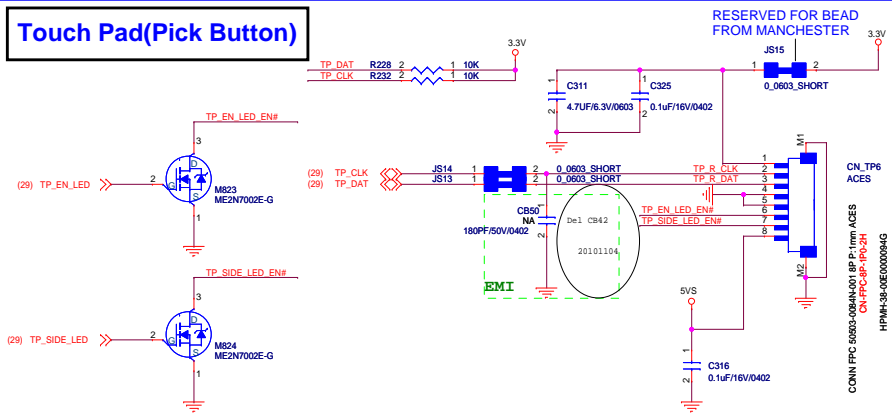
Peak 200mW 40mA



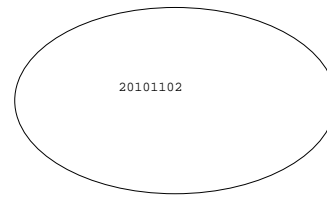
## Finger Print



### Touch Pad(Pick Button)

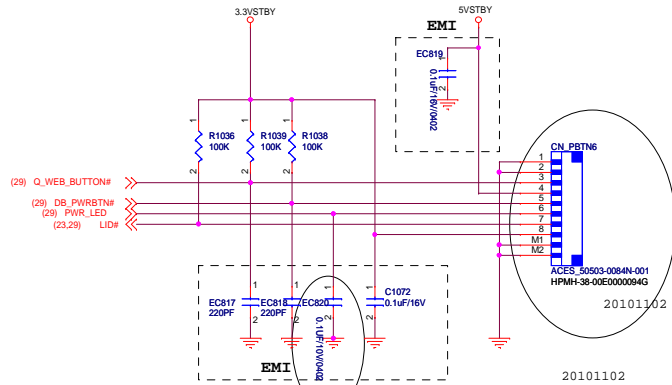


## LID

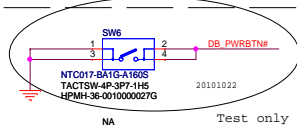




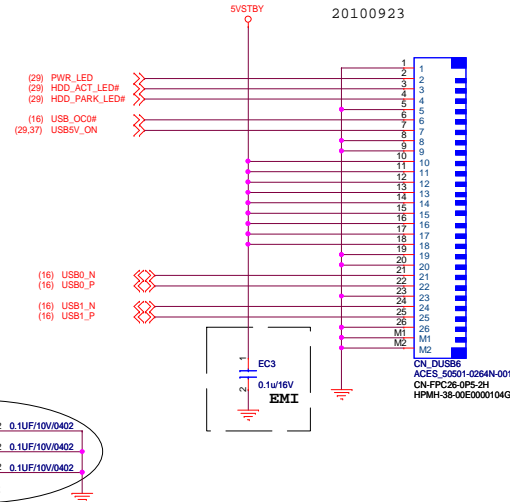
## PWRBTN BOARD



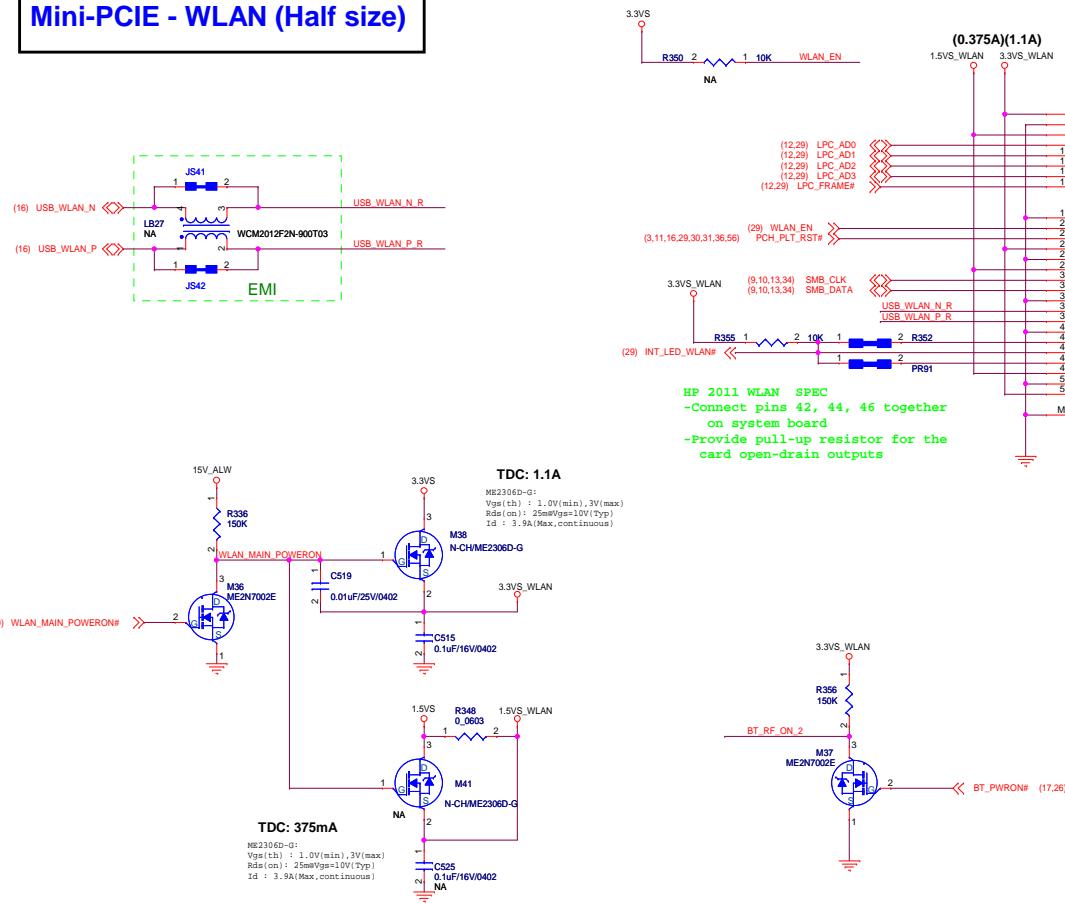
connector on Mother Board for  
Power Button/LED/LID Daughter board



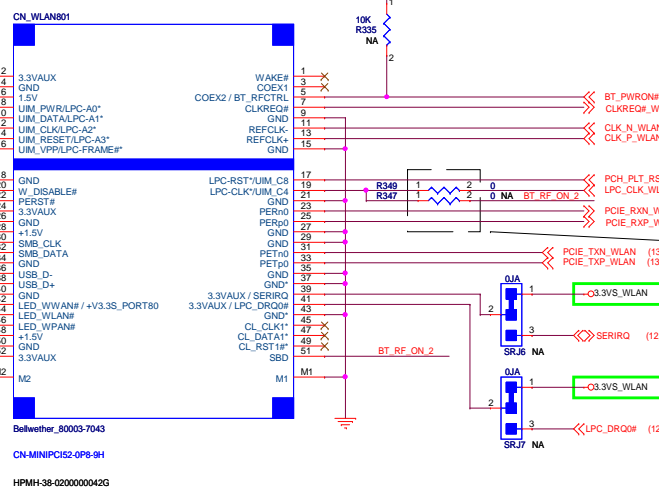
## USB BOARD



## Mini-PCIE - WLAN (Half size)

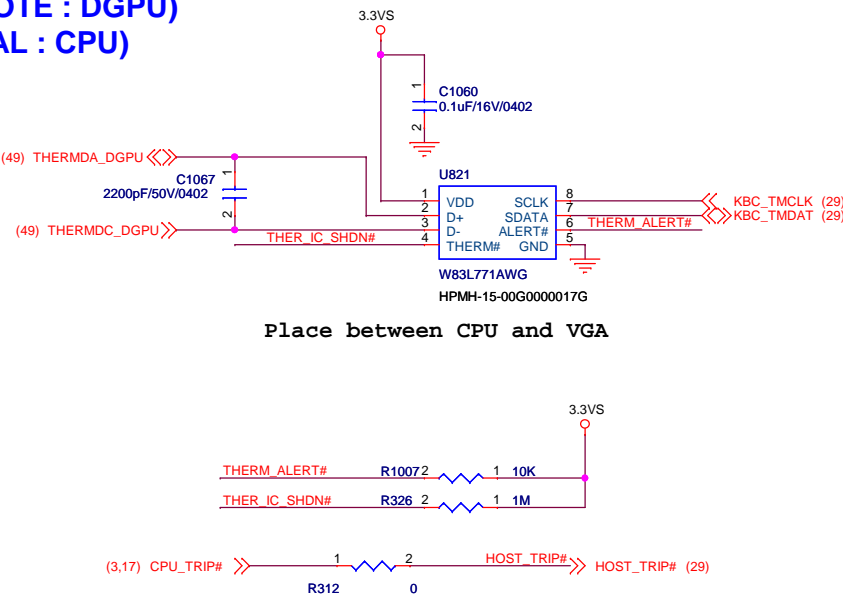


## WLAN CONNECTOR



HP 2011 WLAN SPEC 2nd RF ON/OFF Pin  
Primary path is to implement it on pin 51,  
but 0 Ohm strap to pin 19 required for  
Intel Rainbow Peak ES2 cards use  
(QS will transition to pin 51).

Thermal Sensor  
(REMOTE : DGPU)  
(LOCAL : CPU)

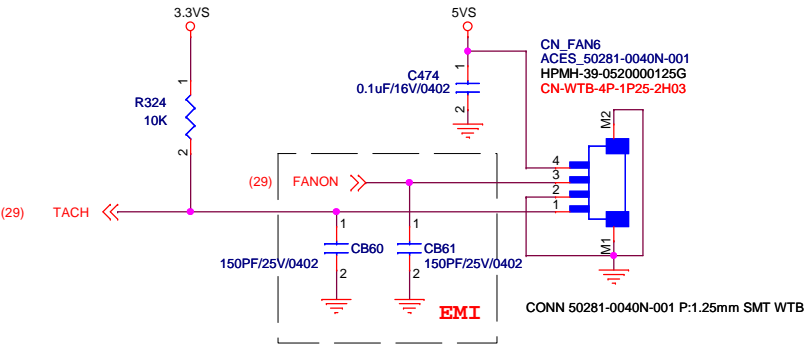


Place between CPU and VGA

THERMAL IC FOR CPU or DGPU

|         |                  |                                      |
|---------|------------------|--------------------------------------|
| WINBOND | W83L771AWG       | ODMH-15-00G0000017G<br>1001100x(98h) |
| ON SEMI | ADT7421ARMZ-REEL | ???                                  |
| GMT     | G780P81U         | ???                                  |

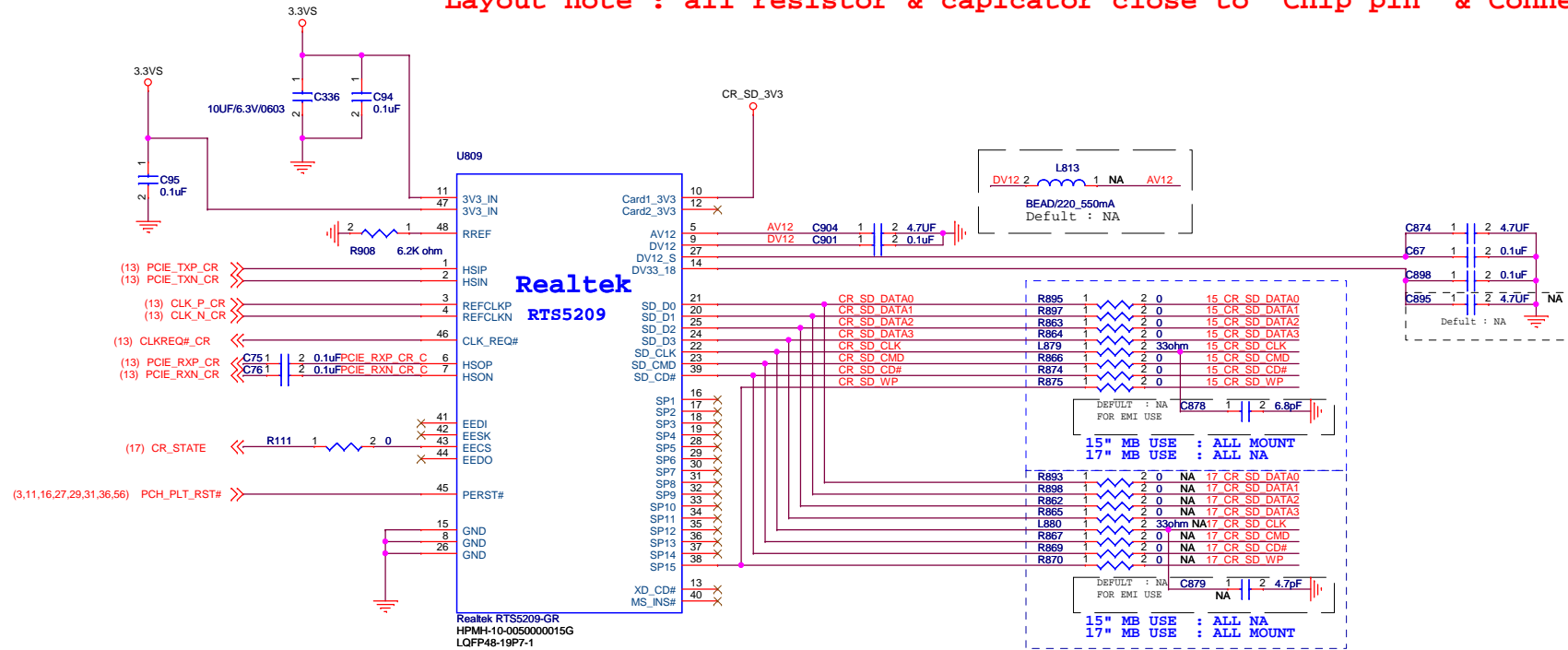
FAN CONN



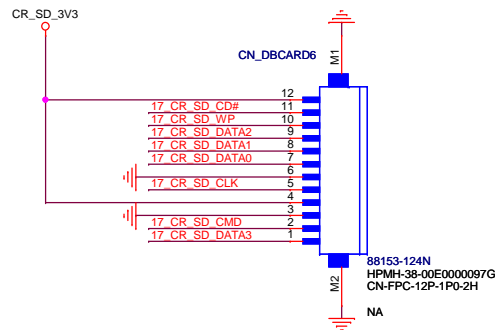


# Card Reader

Layout note : all resistor & capicator close to Chip pin & Connector pin



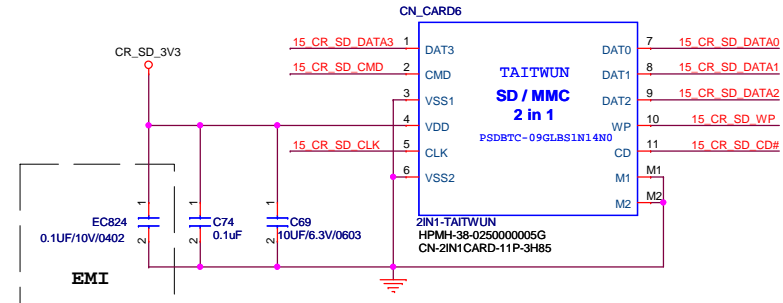
FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA

FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



FOR 15" MB ALL COMPONENT : MOUNT

FOR 17" MB ALL COMPONENT : NA

**FLEX** Computing

|  |                                 |
|--|---------------------------------|
| Project Name :<br>H710DI1                          | Title :<br>Card Reader (R5U220) |
| Size :<br>Document Number :<br>HPMH-40GAB6600-B130 | Rev :<br>B                      |
| Date: Monday, November 08, 2010                    | Sheet : 30 of 63                |



**FLEX** Computing

Project Name :  
**H710DI1**

|         |         |
|---------|---------|
| Title : | RESERVE |
|---------|---------|

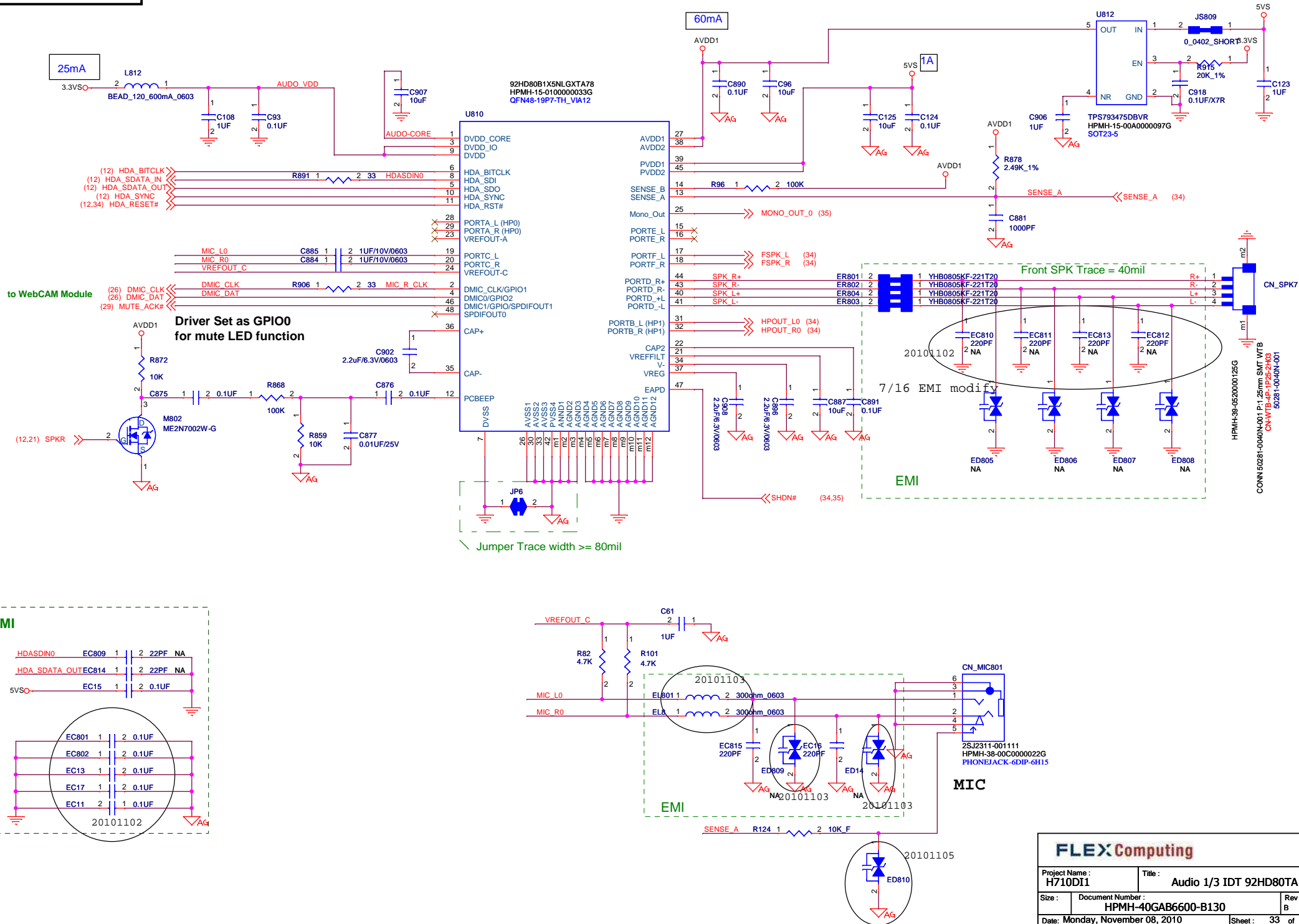
|        |   |
|--------|---|
| Size : | Document Number :<br><b>HPMH-40GAB6600-B130</b> |
|--------|---|

|       |   |
|-------|---|
| Rev : | B |
|-------|---|

Date: Monday, November 08, 2010 Sheet : 32 of 63

Sheet : 32 of 63

# Audio CODEC



**FLEX Computing**

|                                  |   |  |  |
|----------------------------------|---|--|--|
| Project Name :<br><b>H710D11</b> |   | Title :<br><b>Audio 1/3 IDT 92HD80TA</b> |  |
| Size :                           | Document Number :<br><b>HPMH-40GAB6600-B130</b> | Rev :<br><b>B</b>                        |  |
| Date : Monday, November 08, 2010 |   | Sheet : 33 of 63                         |  |





If without supply Woofer all page NA

## WOOFER AMP

HPA00836PWPR  
HTSSOP28-25P6X220-TH

HPA00836PWPR  
28PIN

|      |      |           |
|------|------|-----------|
| G1=0 | G0=0 | GAIN=20dB |
| G1=0 | G0=1 | GAIN=26dB |
| G1=1 | G0=0 | GAIN=32dB |
| G1=1 | G0=1 | GAIN=36dB |

Kevin modify-0909

**FLEX** Computing

|                |         |
|----------------|---------|
| Project Name : | H710DI1 |
|----------------|---------|

|         |                      |
|---------|----------------------|
| Title : | Audio 3/3 WOOFER AMP |
|---------|----------------------|

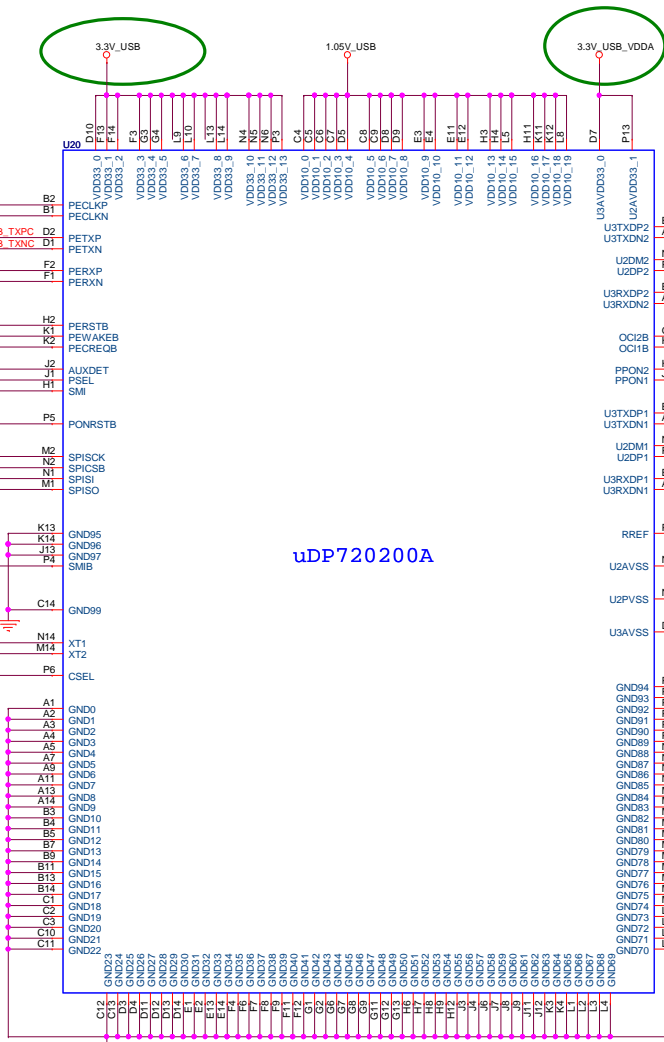
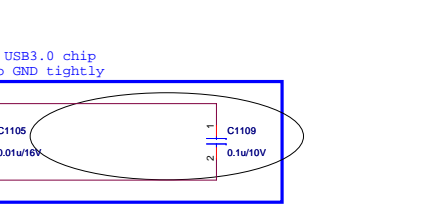
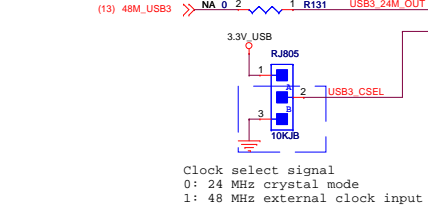
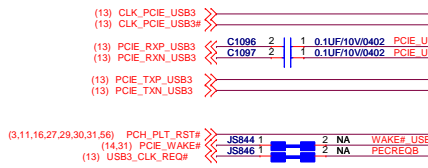
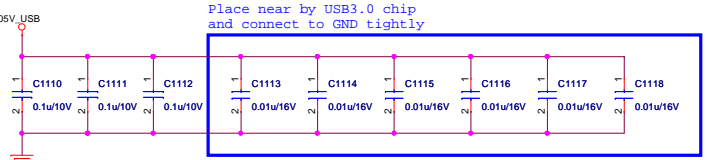
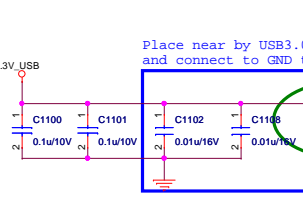
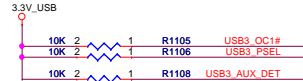
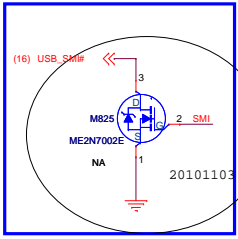
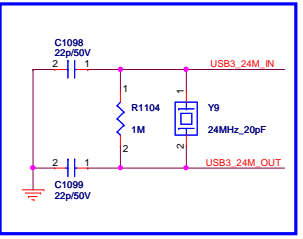
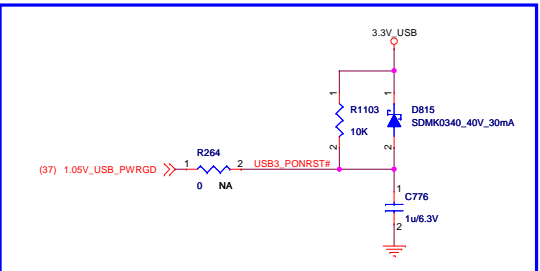
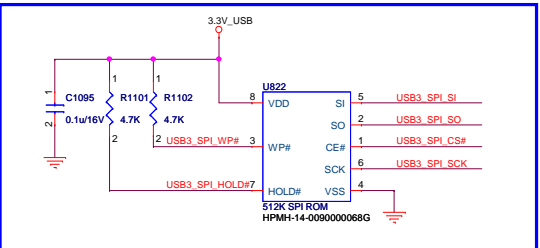
|        |   |
|--------|---|
| Size : | Document Number :<br><b>HPMH-40GAB6600-B130</b> |
|--------|---|

|      |   |
|------|---|
| Rev: | B |
|------|---|

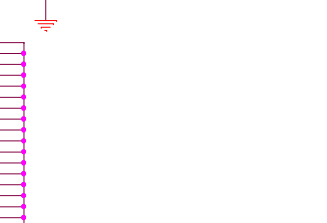
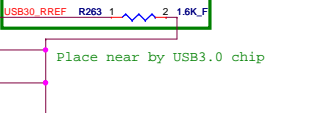
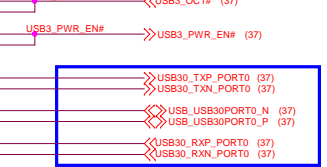
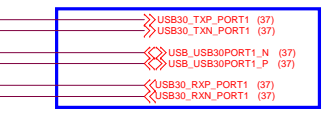
Date: Monday, November 08, 2010

Sheet : 35 of 63

USB3.0 NEC uDP720200



HPMH-10-00C0000024G  
IC uDP720200AF1 USB3.0 FBGA-176  
NEC\_uDP720200A

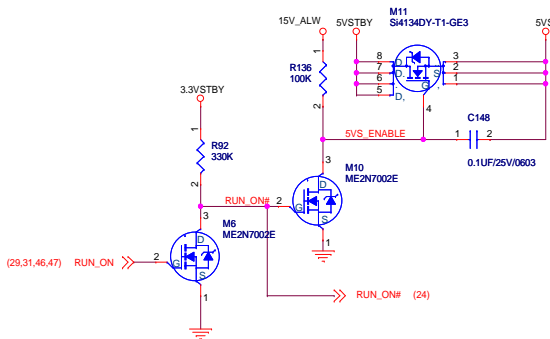


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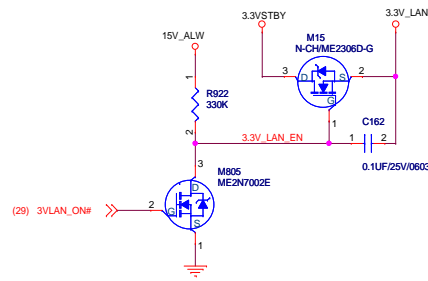
|                                  |                   |                          |         |
|----------------------------------|-------------------|--------------------------|---------|
| Project Name : H710D11           |                   | Title : USB3.0_uDP720200 |         |
| Size :                           | Document Number : | HPMH-40GAB6600-B130      | Rev : B |
| Date : Monday, November 08, 2010 |                   | Sheet : 36 of 63         |         |



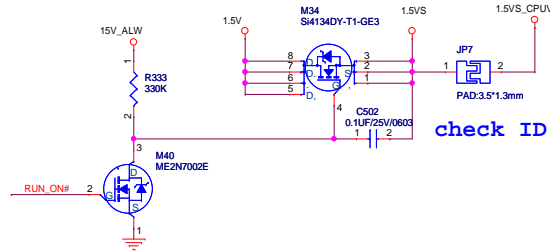




TDC: ?A



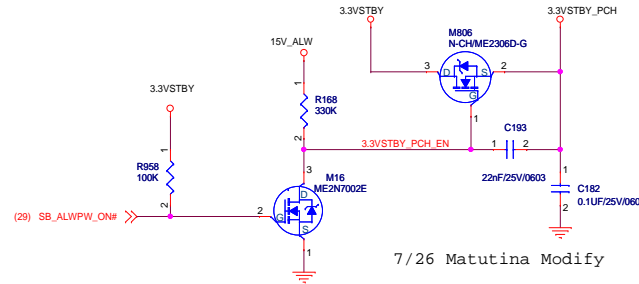
TDC: 0.3A



TDC: ?A

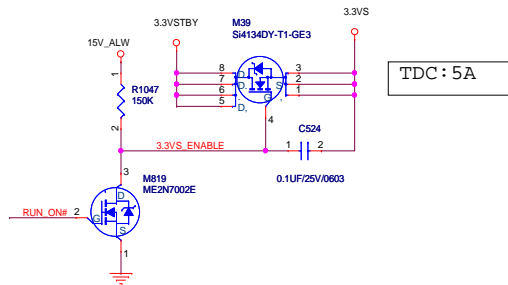
check ID

ME4626 :  
Vgs(th): 3V(max)  
Rds(on): 3.2m@Vgs = 10V (Max)  
Rds(on): 4.9m@Vgs = 4.5V (Max)  
Id : 23A



TDC: 0.6A

7/26 Matutina Modify



TDC: 5A

ME2306D:

Vgs(th) : 1.0V(min),3.0V(max)  
Rds(on) : 31m @ Vgs = 10V(MAX)  
Rds(on) : 52m @ Vgs = 4.5V(MAX)  
Id : 3.9A(Max)

ME4894-G:

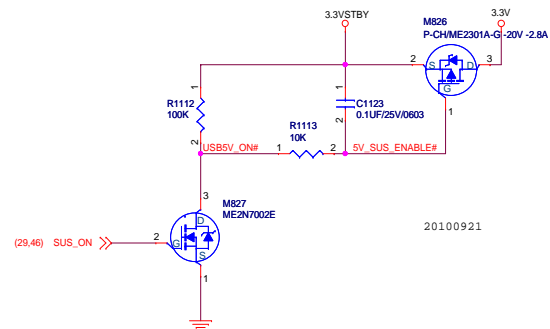
Vgs(th) : 1.0V(min),3.0V(max)  
Rds(on) : 11.7m @ Vgs = 10V (MAX)  
Rds(on) : 18.2m @ Vgs = 4.5V(MAX)  
Id : 11.5A(Max)

ME2301A:

Vgs(th) : -0.9V(max)  
Rds(on) : 75m @ Vgs = -4.5V(MAX)  
Id : -2.8A(Max)

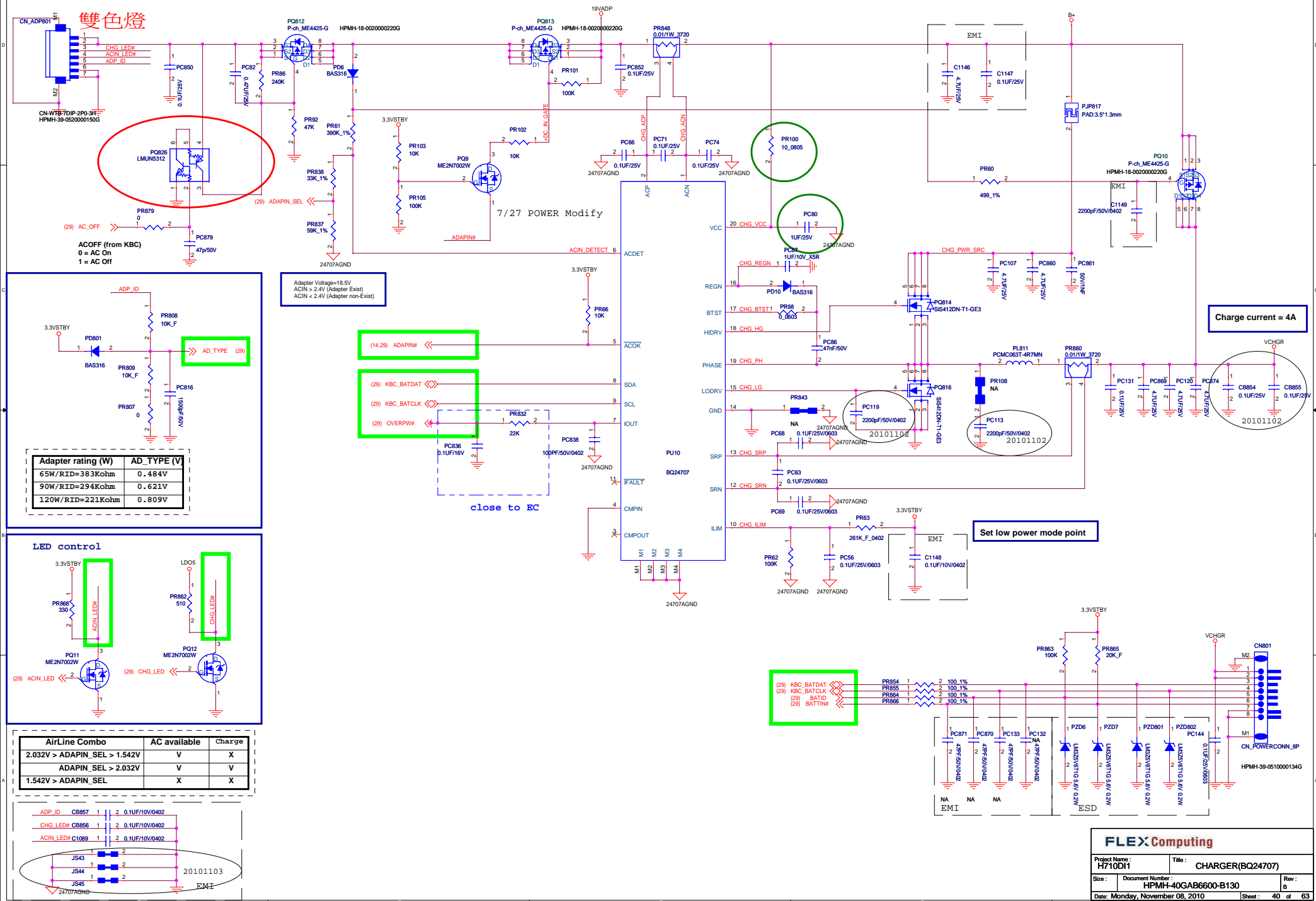
3.3V

500mW / 3.3V



20100921

# Charger





5V / 3.3VSTBY

Freq=300KHz  
TDC = 7 A  
OCP = 10 A

\* Options 1.  
5VSTBY

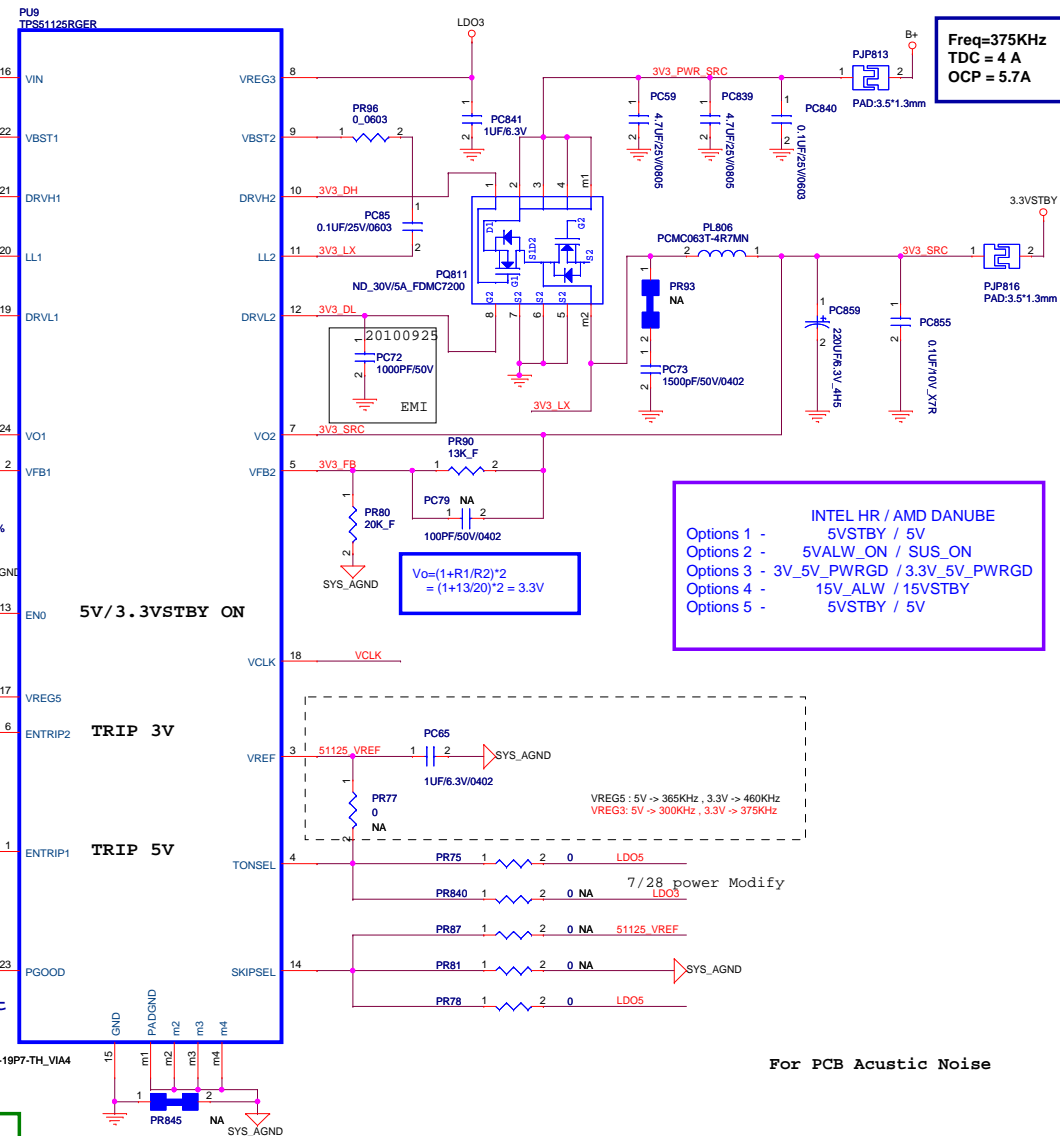
\* Options 2.

\* Options 3.  
(38) 3V\_5V\_PWRGD

Table 3. Enabling State

| EN0      | ENTRIP1    | ENTRIP2    | VREF | VREG5 | VREG3 | CH1 | CH2 | VCLK |
|----------|------------|------------|------|-------|-------|-----|-----|------|
| GND      | Don't Care | Don't Care | Off  | Off   | Off   | Off | Off | Off  |
| R to GND | Off        | Off        | On   | On    | On    | Off | Off | Off  |
| R to GND | On         | Off        | On   | On    | On    | On  | Off | Off  |
| R to GND | Off        | On         | On   | On    | On    | Off | On  | Off  |
| R to GND | On         | On         | On   | On    | On    | On  | On  | Off  |
| Open     | Off        | Off        | On   | On    | On    | Off | Off | Off  |
| Open     | On         | Off        | On   | On    | On    | On  | Off | On   |
| Open     | Off        | On         | On   | On    | On    | Off | On  | Off  |
| Open     | On         | On         | On   | On    | On    | On  | On  | On   |

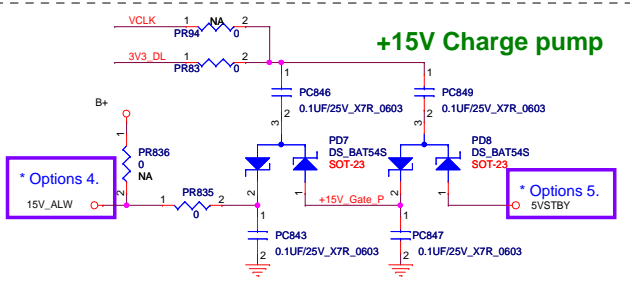
PU3-m1  
For layout request, no connect anything.



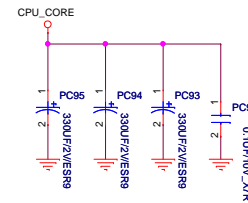
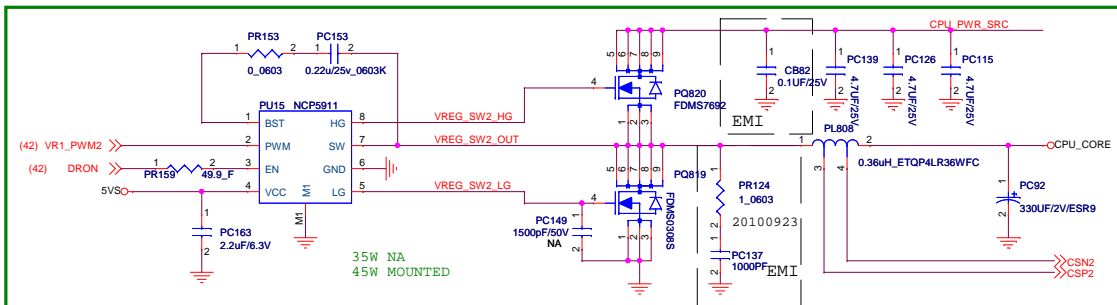
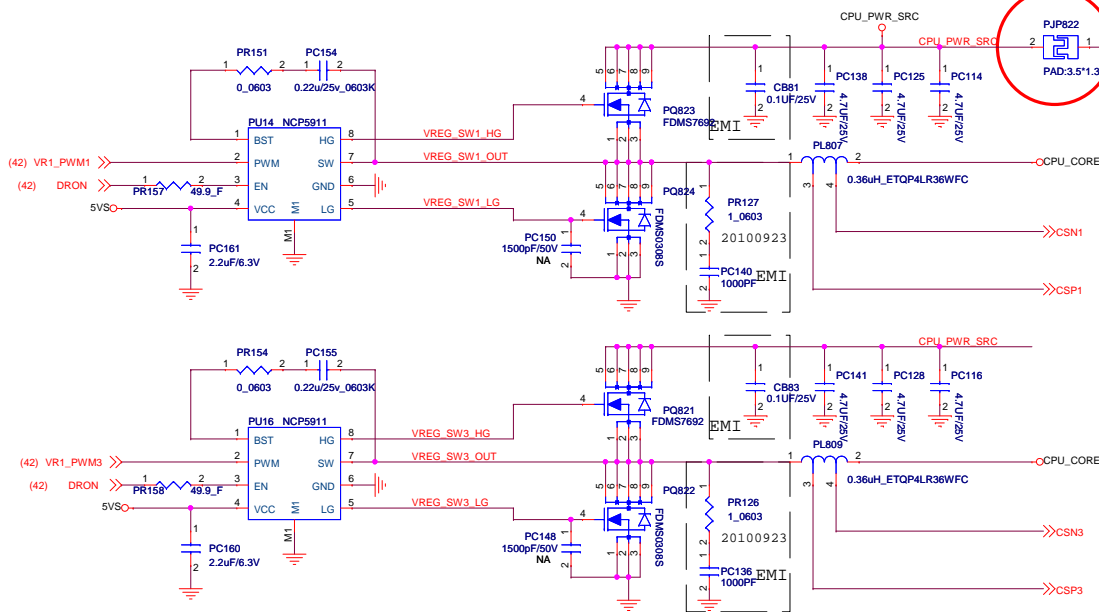
Freq=375KHz  
TDC = 4 A  
OCP = 5.7 A

INTEL HR / AMD DANUBE  
Options 1 - 5VSTBY / 5V  
Options 2 - 5VALW\_ON / SUS\_ON  
Options 3 - 3V\_5V\_PWRGD / 3.3V\_5V\_PWRGD  
Options 4 - 15V\_ALW / 15VSTBY  
Options 5 - 5VSTBY / 5V

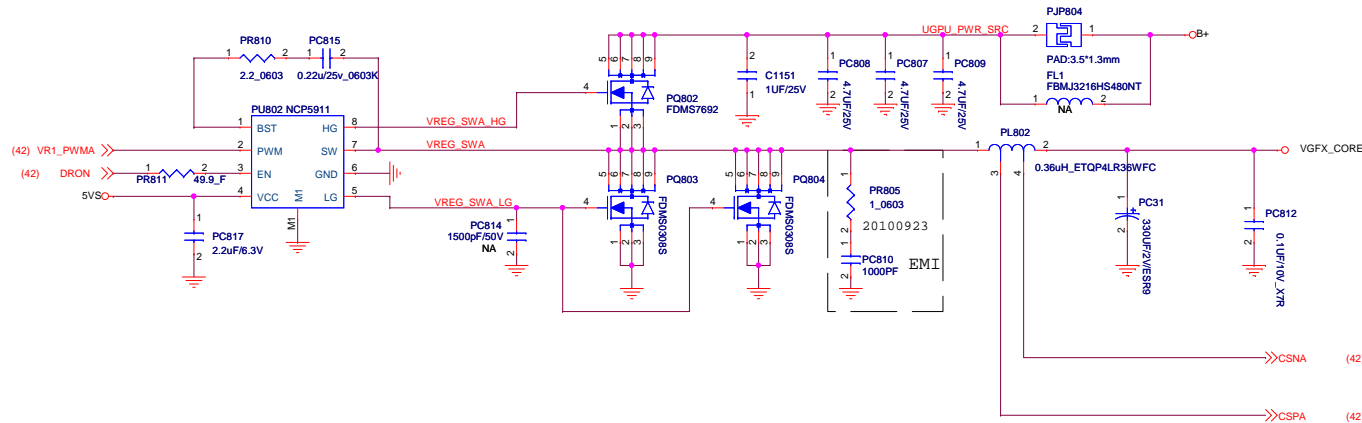
For PCB Acoustic Noise







| Vcore setting Table |                 |               |                      |
|---------------------|-----------------|---------------|----------------------|
|                     | 45W             | 35W           |                      |
| Reference           | SV-QC           | SV-DC         | For 35W component PN |
| PU15                | NCP5911         | NA            |                      |
| PR153               | 0_0603_5%       | NA            |                      |
| PC153               | 0.22UF_25V_0603 | NA            |                      |
| PR159               | 49.9_0402_1%    | NA            |                      |
| PC163               | 2.2UF_6.3V_0603 | NA            |                      |
| PQ820               | FDMS7692        | NA            |                      |
| PQ819               | FDMS0308S       | NA            |                      |
| PL808               | 0.36uH          | NA            |                      |
| PR874               | 73.2K_0402_1%   | 41.2K_0402_1% | HPMH-30-141221-990G  |
| PR861               | 24K_0402_1%     | 24.9K_0402_1% | HPMH-30-124921-990G  |
| PR867               | 21K_0402_1%     | 12.4K_0402_1% | HPMH-30-112421-990G  |



1.05VS\_VCCIO  
1.05VS

(38,45) 1.05VS\_PWRGD

(38,46) 1.05V\_VCCIO\_EN

$$I_{OCP} = ((PR4551 * 10) / 8 * R_{ds(on)}) + I_{O(max)} / 6 = 18.4A$$

Freq=430KHz

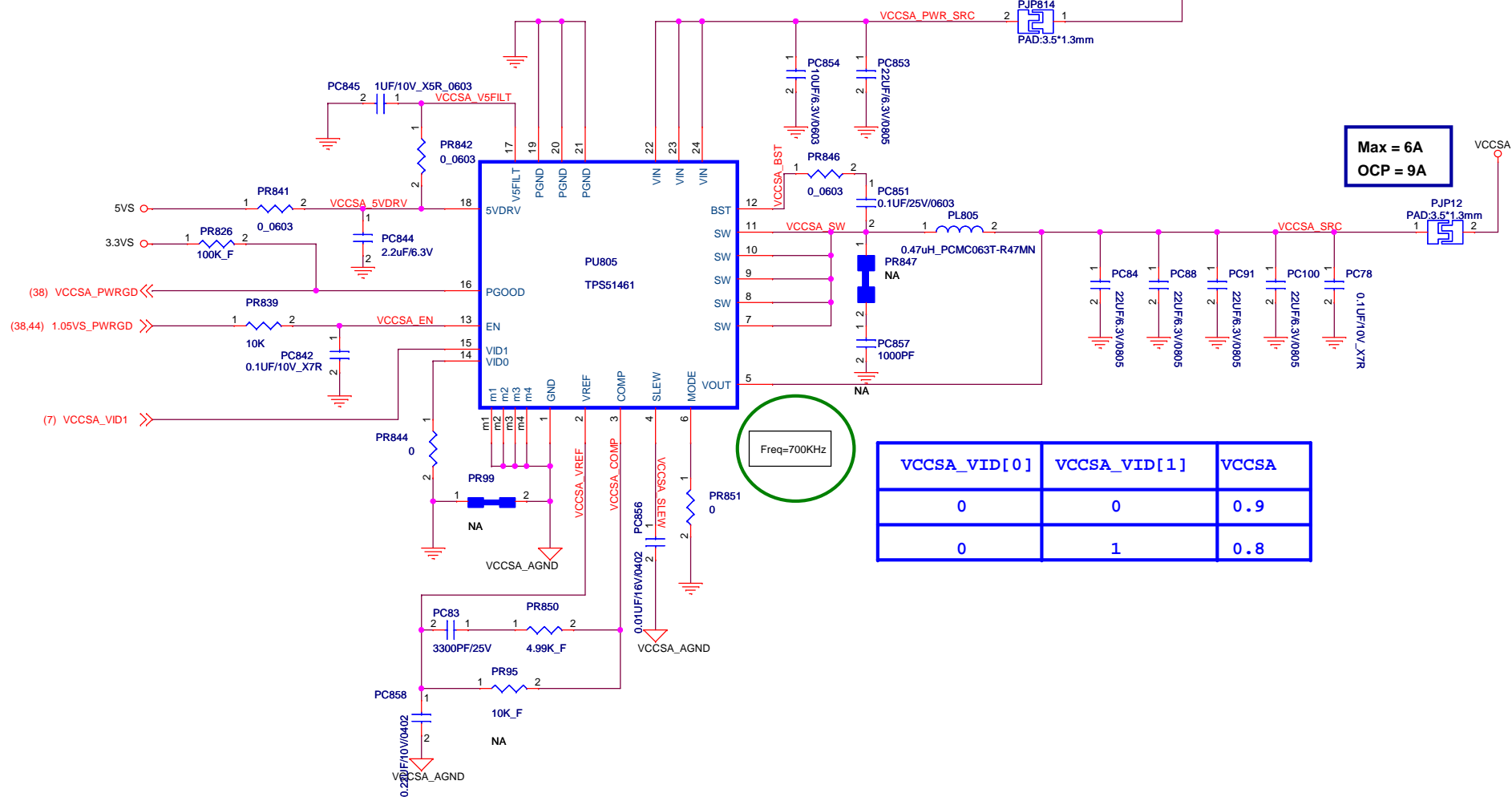
RF pull down to GND with resistor : Auto-skip  
RF connect to PGOOD with resistor : Force CCM

TDC=12.87A  
OCP=15.54A

$$V_o = 0.75 * (1 + (PR529 / PR531)) = 0.75 * (1 + 0.47) = 1.107V$$

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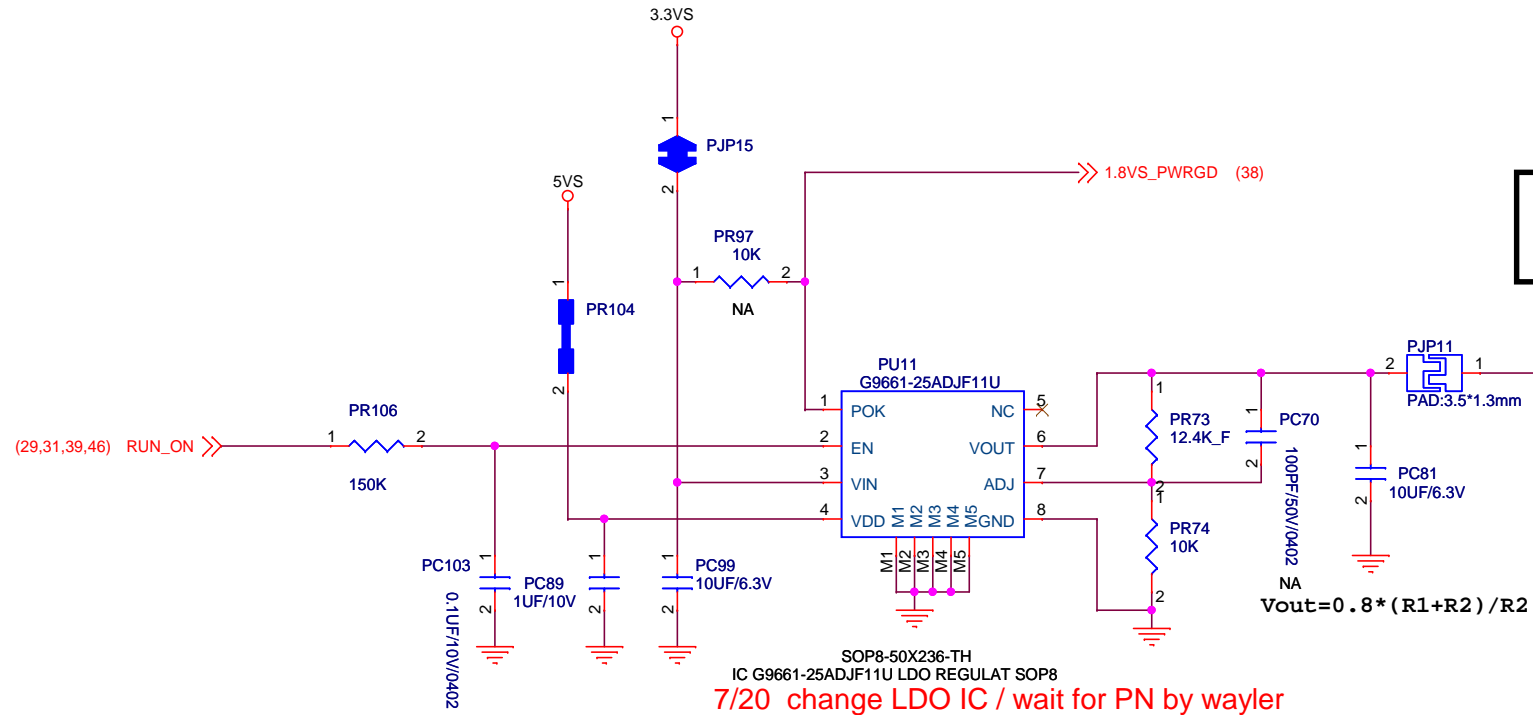
|                                 |  |                             |            |
|---------------------------------|--|-----------------------------|------------|
| Project Name :<br>H710DI1       |  | Title :<br>1.05VS(TPS51218) |            |
| Size :<br>Custom                | Document Number :<br>HPMH-40GAB6600-B130 |                             | Rev :<br>B |
| Date: Monday, November 08, 2010 |  | Sheet : 44 of 63            |            |

**VCCSA**

| VCCSA_VID[0] | VCCSA_VID[1] | VCCSA |
|--------------|--------------|-------|
| 0            | 0            | 0.9   |
| 0            | 1            | 0.8   |



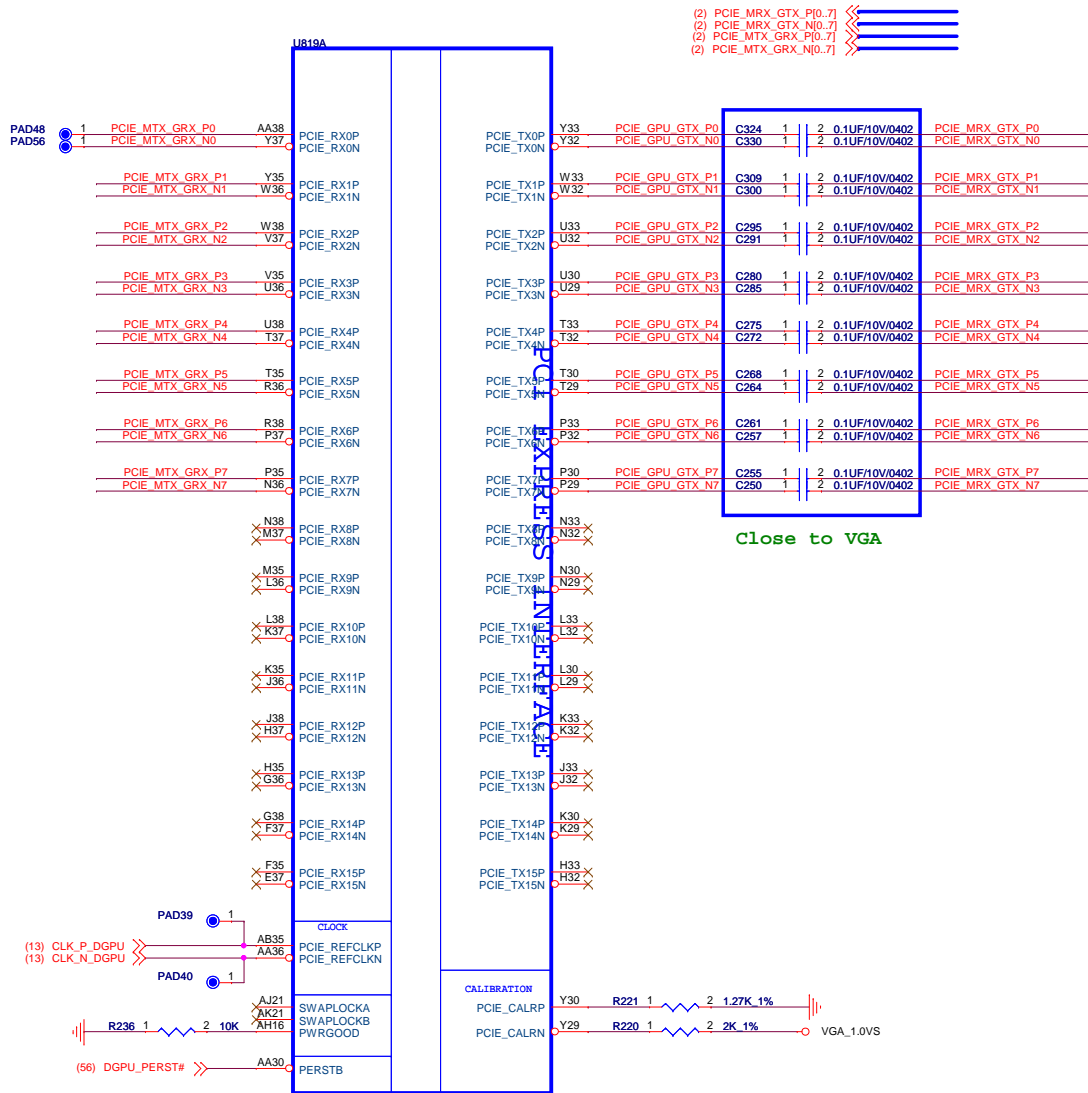
1.8VS



FLEX Computing

|                                 |  |                  |            |
|---------------------------------|--|------------------|------------|
| Project Name :<br>H710DI1       |  | Title :<br>1.8VS |            |
| Size :                          | Document Number :<br>HPMH-40GAB6600-B130 |                  | Rev :<br>B |
| Date: Monday, November 08, 2010 |  | Sheet : 47 of 63 |            |



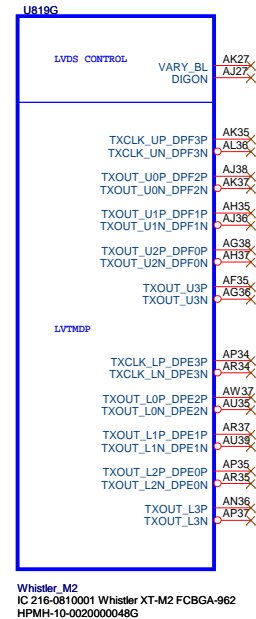


Whistler\_M2  
IC 216-0810001 Whistler XT-M2 FCBGA-962  
HPMH-10-0020000048G

| GPU TYPE    | PN                  |
|-------------|---------------------|
| Whistler XT | HPMH-10-0020000048G |
| Seymour-XT  | HPMH-10-0020000049G |

(2) PCIE\_MRX\_GTX\_P0[0..7]  
(2) PCIE\_MRX\_GTX\_N0[0..7]  
(2) PCIE\_MTX\_GRX\_P0[0..7]  
(2) PCIE\_MTX\_GRX\_N0[0..7]

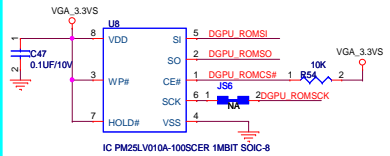
Close to VGA



Whistler\_M2  
IC 216-0810001 Whistler XT-M2 FCBGA-962  
HPMH-10-0020000048G

For del vBIOS ROM design:  
1.P49 -U8,C47,R54  
2.P53 -R1001,R1002,R1015

#### For GDDR5 used



NA for del vBIOS ROM design.

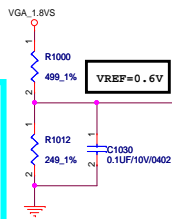
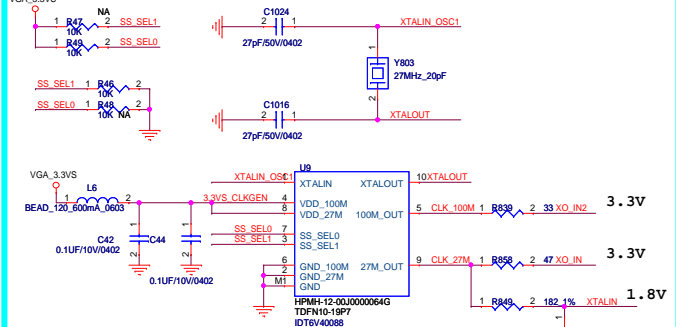
#### VMEM\_ID

|   | DVPPDATA_2 | DVPPDATA_1 | DVPPDATA_0 |
|---|------------|------------|------------|
| Seymour Hynix H5GQ2H24MFR-T2C (128Mx16) x4pcs   | 0          | 0          | 0          |
| Seymour Samsung K4G20325FC-HC04 (128Mx16) x4pcs | 0          | 0          | 1          |
| Whistler Hynix H5GQ1H24AFR-T2C (64Mx16) x8pcs   | 0          | 1          | 0          |
| Whistler Samsung K4G10325FE-HC04 (64Mx16) x8pcs | 0          | 1          | 1          |
| Seymour Hynix H5GQ1H24AFR-T2C (64Mx16) x4pcs    | 1          | 0          | 0          |
| Seymour Samsung K4G10325FE-HC04 (64Mx16) x4pcs  | 1          | 0          | 1          |
| Seymour Elpida EDW2032BABG-50-F(128Mx16) x4pcs  | 1          | 0          | 1          |
| Whistler Elpida EDW1032BABG-50-F(64Mx16) x8pcs  | 1          | 1          | 1          |

#### 100 MHz Spread Selection Table

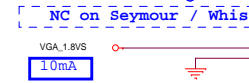
| PIN3 | PIN7 | PIN5  | Down Spread% |
|------|------|-------|--------------|
| S1   | S0   |       | Down Spread% |
| L    | L    | OFF   |              |
| L    | M    | -0.5  |              |
| L    | H    | -2.5  |              |
| M    | M    | -0.25 |              |
| M    | L    | -0.75 |              |
| M    | H    | -1.0  |              |
| H    | L    | -1.5  |              |
| H    | M    | -2.0  | Default      |
| H    | H    | -3.0  |              |

Have 1M resistor in IDT6V4088



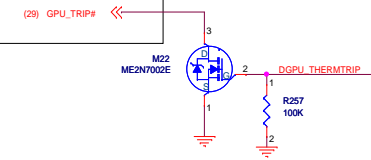
(28) THERMADA, DGPU

(28) THERMDC, DGPU

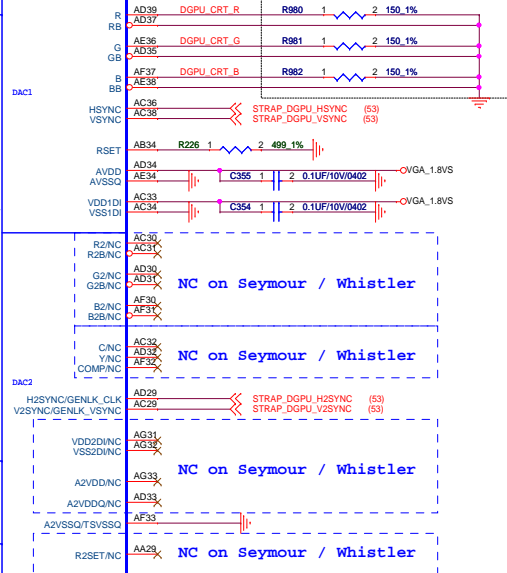


Whistler\_M2  
IC 216-0810001 Whistler XT-M2 FCBGA-962  
HPMH-10-0020000048G

OD, PU is at  
PWRGD circuit

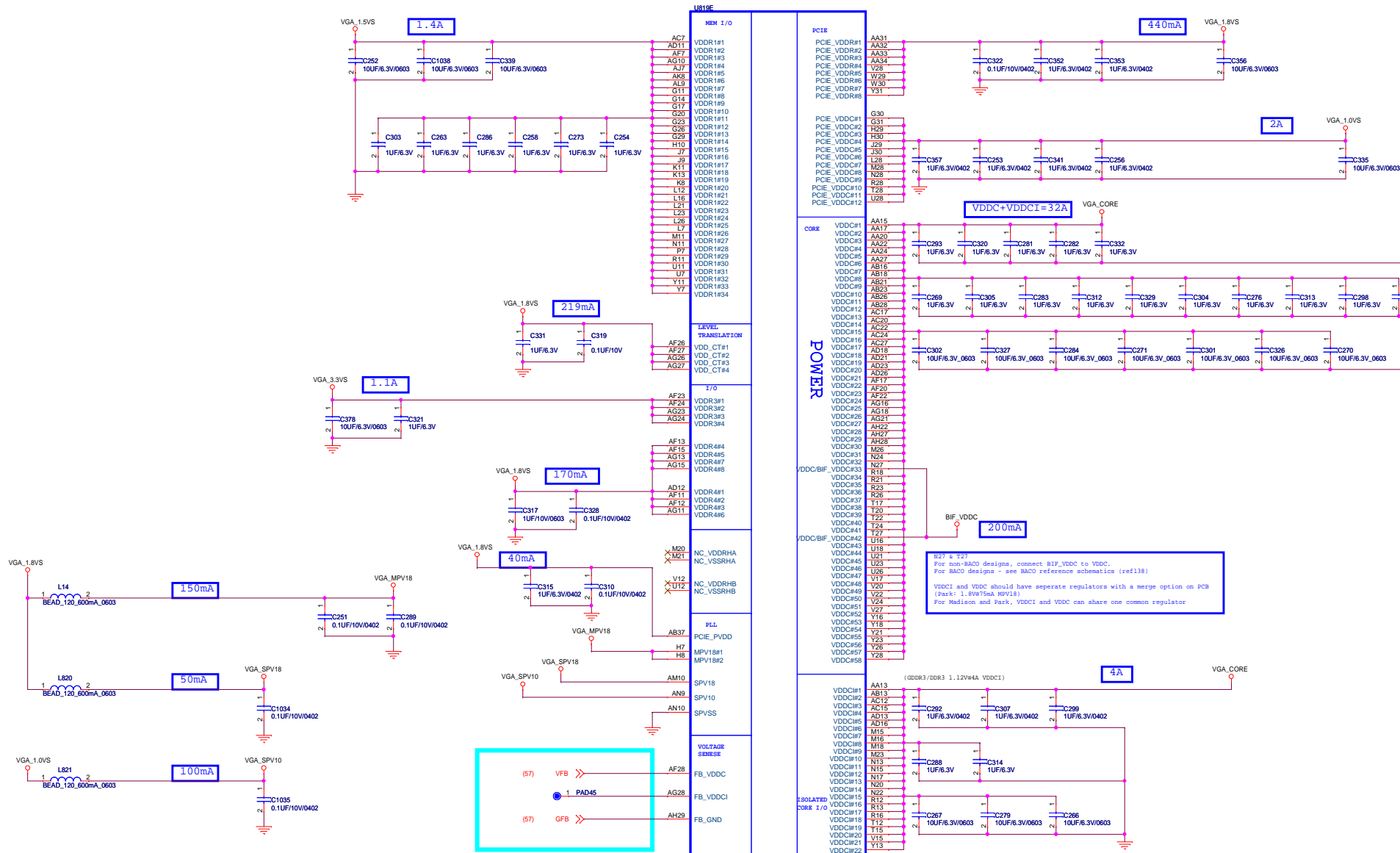


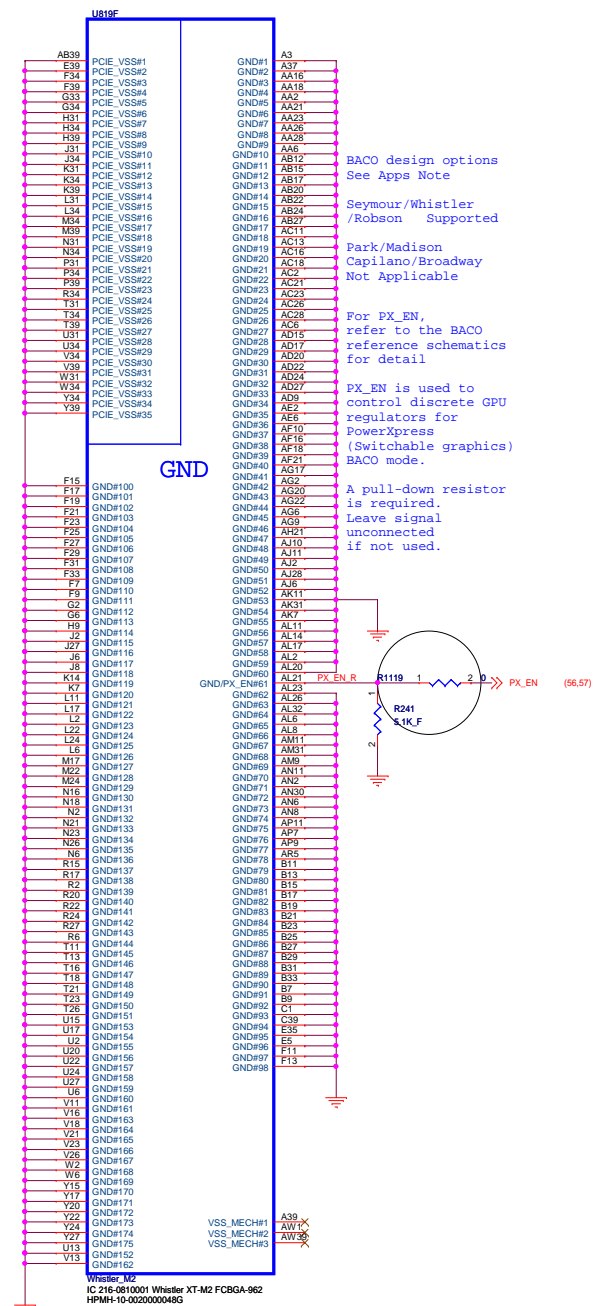
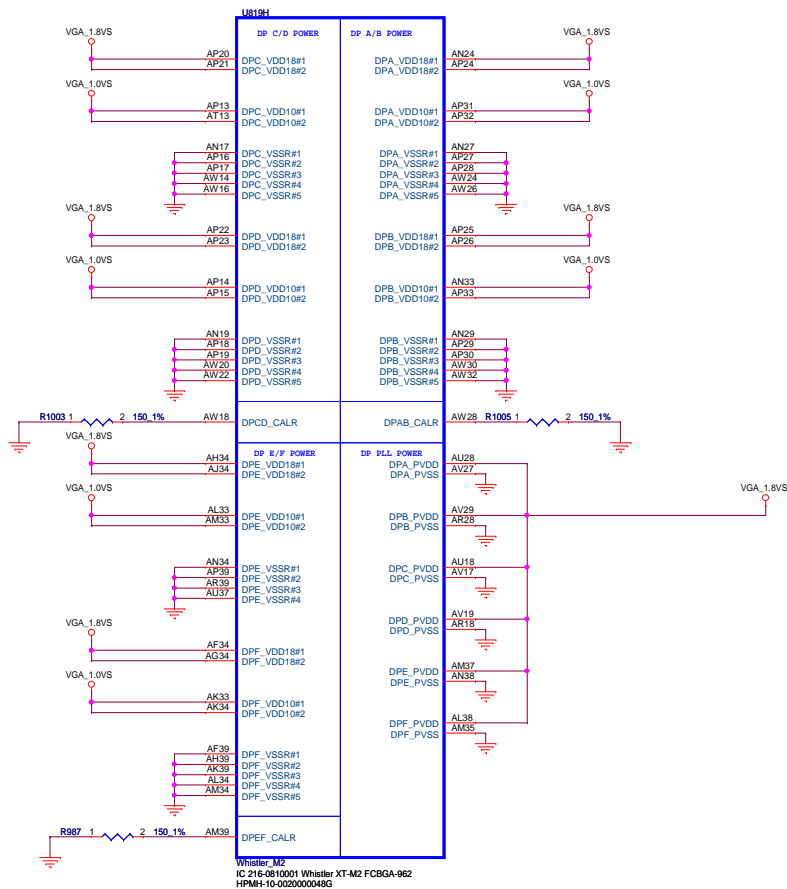
For DGPU debug, mounted  
Close to chipset



For DGPU debug





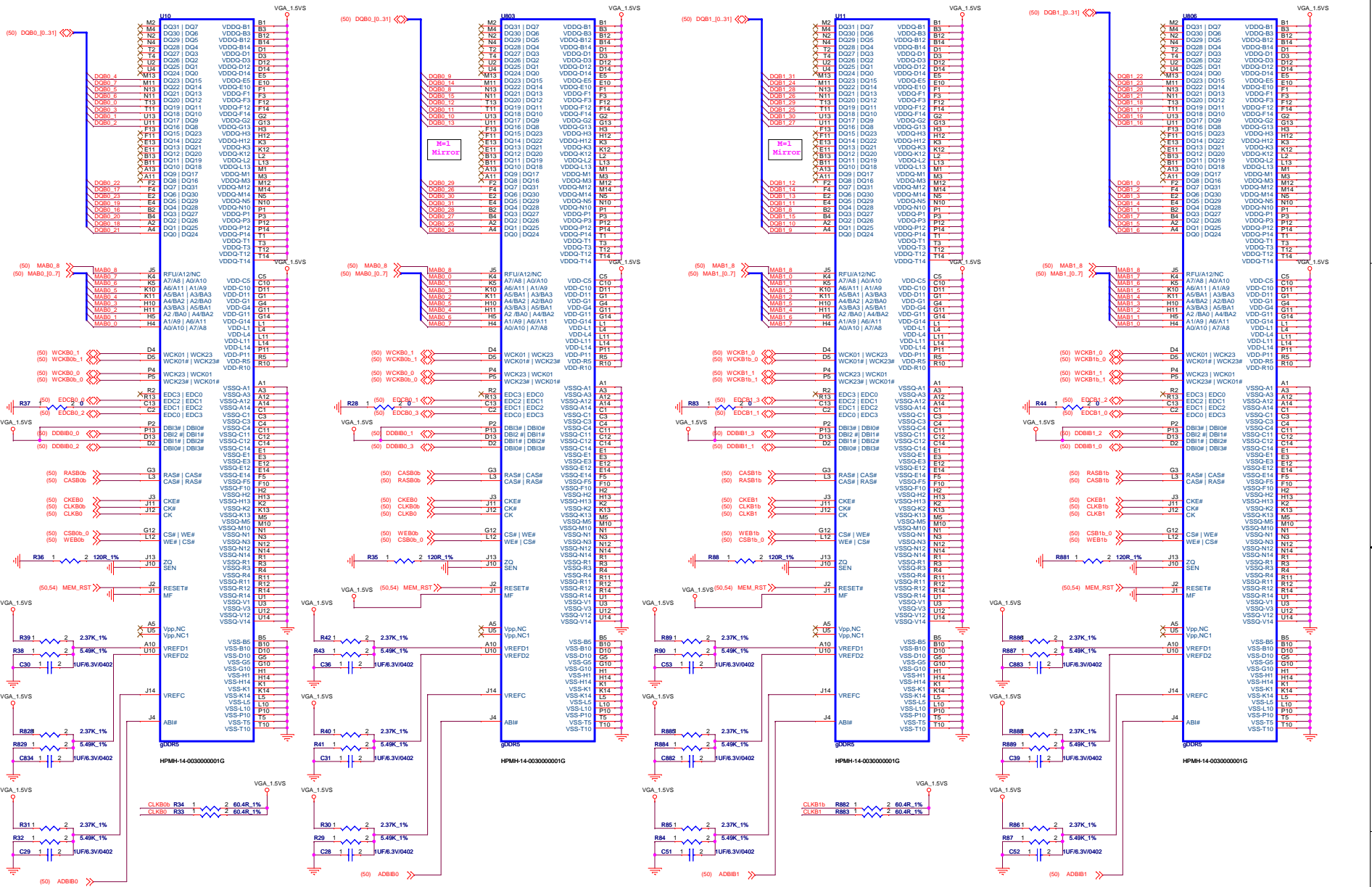




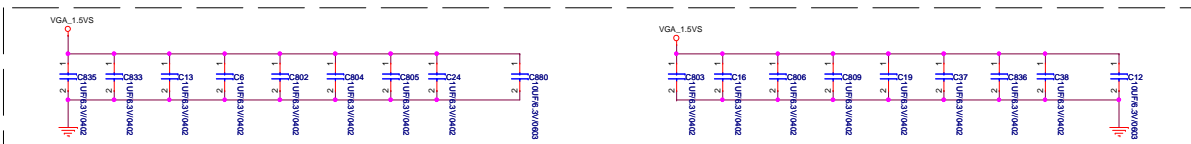








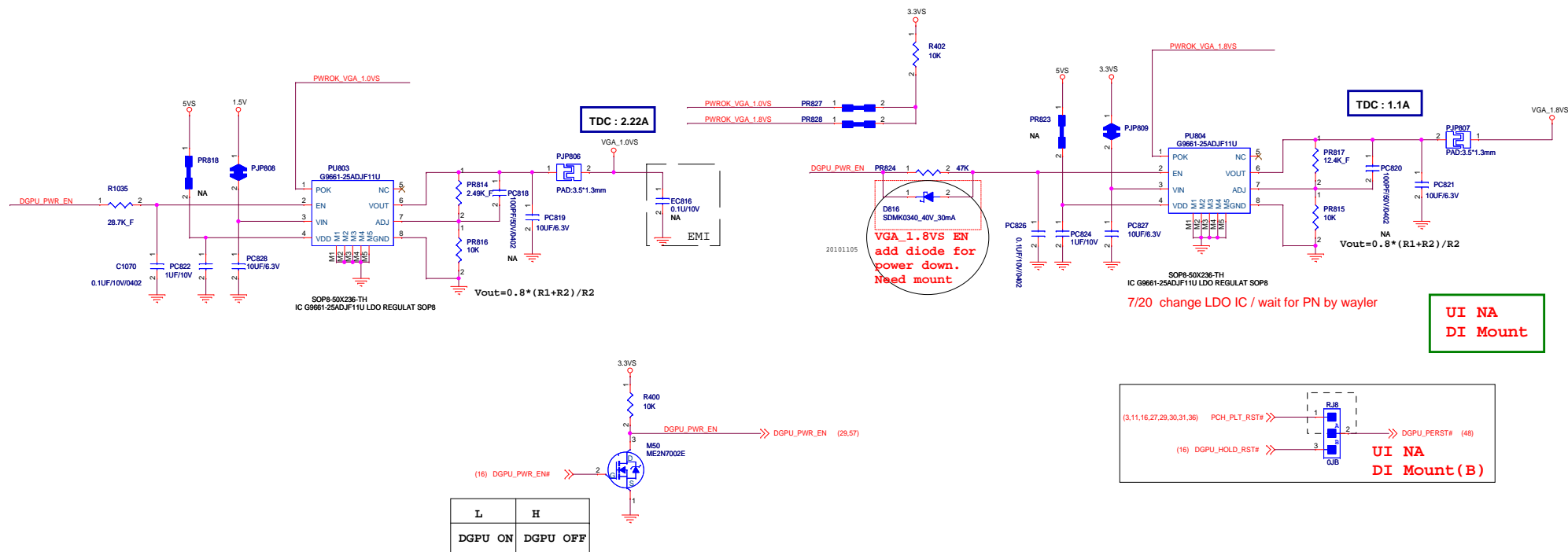
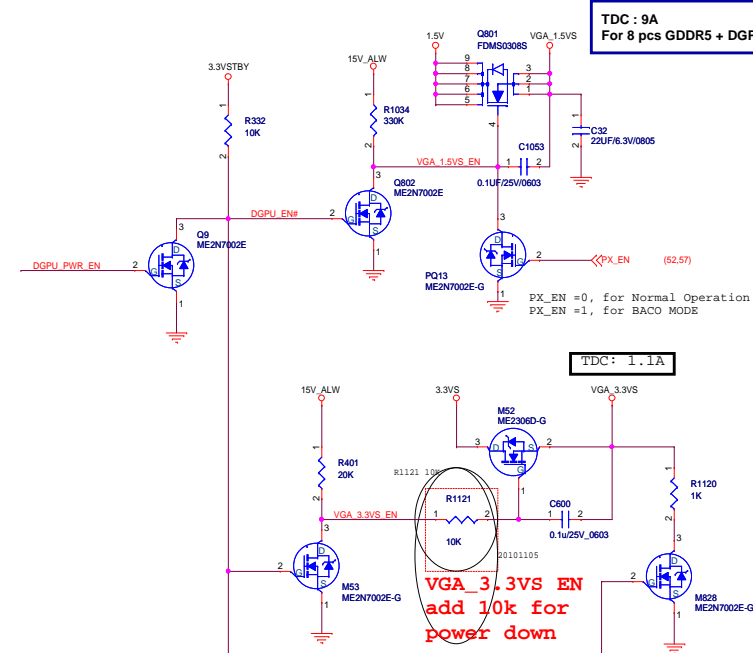
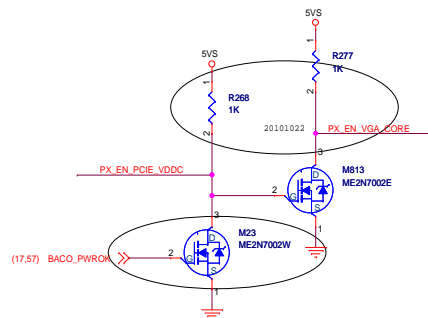
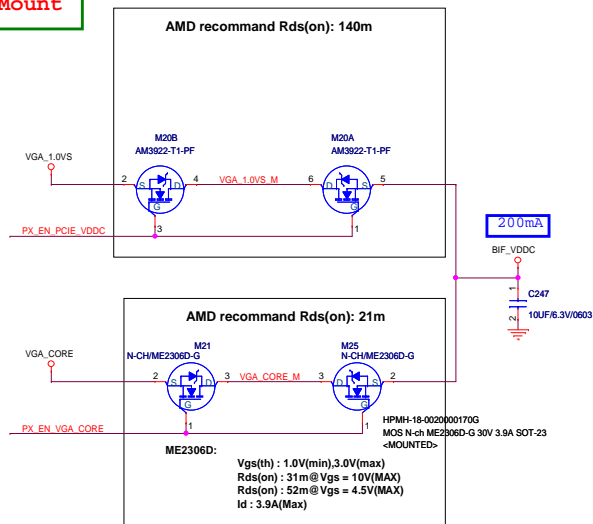
GDDR5 Memory Channel B X16 Mode



Decoupling caps for clamshell configuration:  
 1X 10uF per 2 clamshell DRAM  
 8 X 1uF per 2 clamshell DRAM

UI NA  
DI Mount

TDC : 9A  
For 8 pcs GDDR5 + DGPU



UI NA  
DI Mount

Diagram illustrating the UI NA DI Mount(B) component and its connections:

- Inputs:**
  - PCH\_PLT\_RST#** (Signals: 3,11,16,27,29,30,31,36) connected to Pin 1 of the top RJ8.
  - DGPU\_HOLD\_RST#** (Signal: 16) connected to Pin 3 of the bottom RJ8.
- Output:**
  - DGPU\_PERST# (48)** connected to Pin 2 of the top RJ8.

| VID4 (PP2) (GPIO16) | VID3 (PP1) (GPIO20) | VID2 (PP0) (GPIO15) | VGA_CORE |
|---------------------|---------------------|---------------------|----------|
| 0                   | 0                   | 1                   | 1.05V    |
| 1                   | 0                   | 0                   | 0.900V   |

| VID |   |   |   |   |   | V <sub>DAC</sub> (V) |
|-----|---|---|---|---|---|----------------------|
| 6   | 5 | 4 | 3 | 2 | 1 | 0                    |
| 0   | 1 | 0 | 0 | 1 | 0 | 0                    |
| 0   | 1 | 1 | 0 | 0 | 0 | 0                    |

5VS PU maybe leakage in BACO. Change to VGA\_3.3VS

(49) PWRPLAY\_VID2  
(49) PWRPLAY\_VID1  
(49) PWRPLAY\_VID0

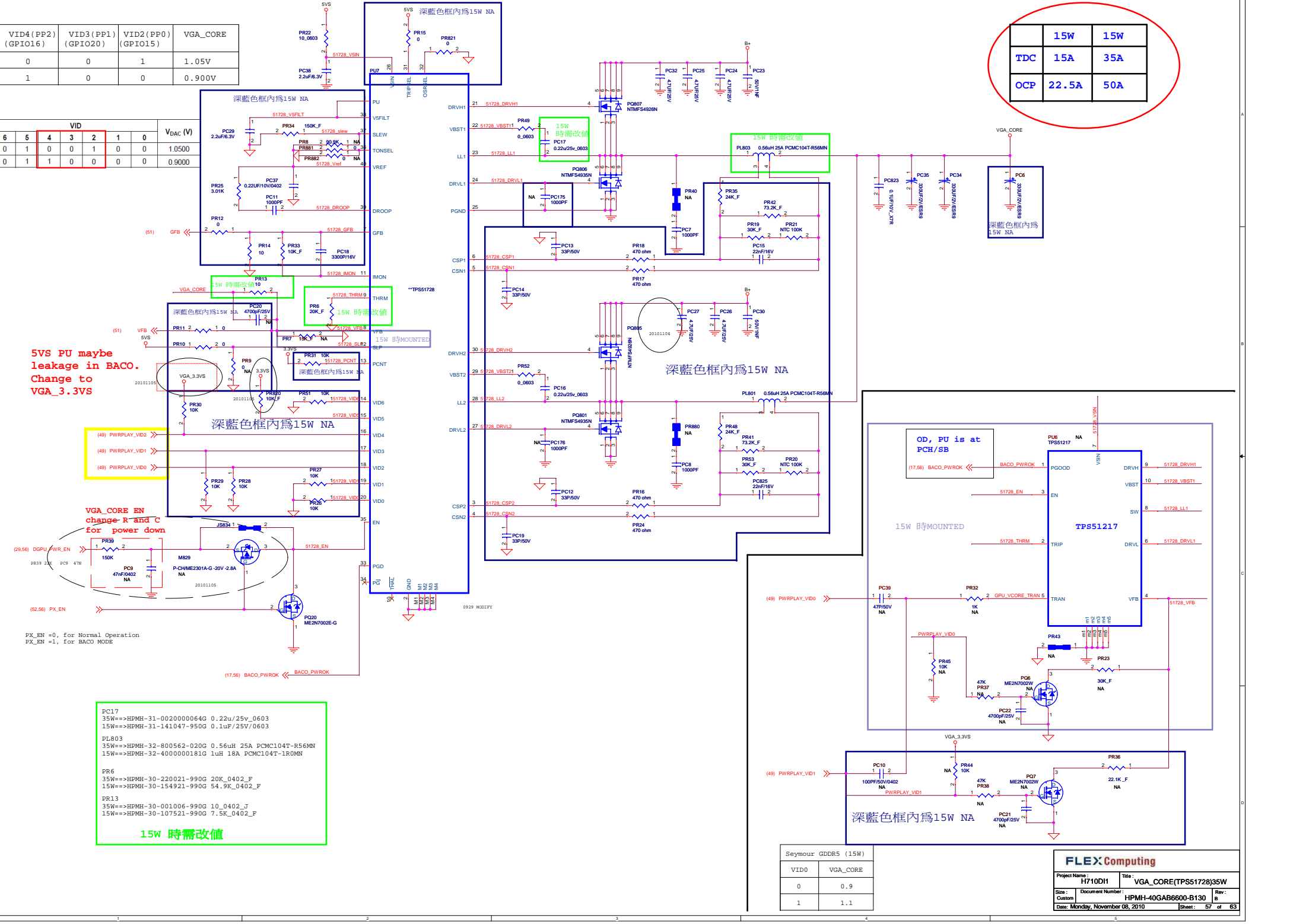
VGA\_CORE EN change R and C for power down

(29.56) DGPU\_PWR\_EN

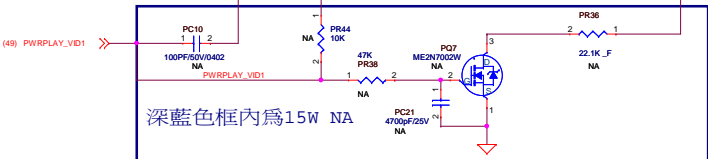
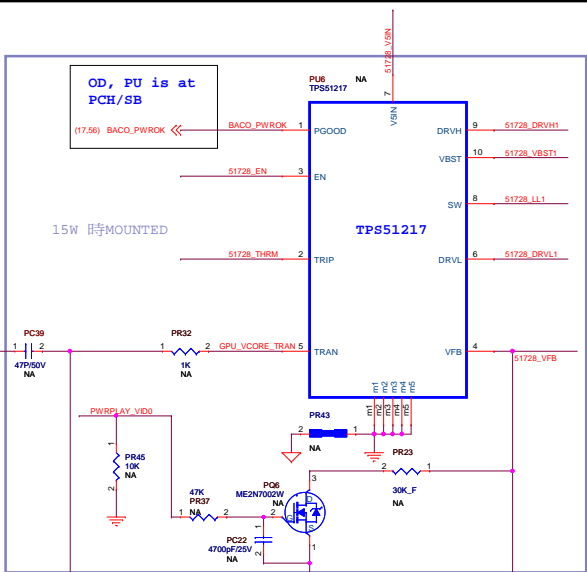
PX\_EN = 0, for Normal Operation  
PX\_EN = 1, for BACO MODE

PC17  
35W==>HPMH-31-0020000064G 0.22u/25v\_0603  
15W==>HPMH-31-141047-950G 0.1uF/25V/0603  
PL803  
35W==>HPMH-32-800562-020G 0.56uH 25A PCMC104T-R56MN  
15W==>HPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN  
PR6  
35W==>HPMH-30-220021-990G 20K\_0402\_F  
15W==>HPMH-30-154921-990G 54.9K\_0402\_F  
PR13  
35W==>HPMH-30-001006-990G 10\_0402\_J  
15W==>HPMH-30-107521-990G 7.5K\_0402\_F

15W 時需改值

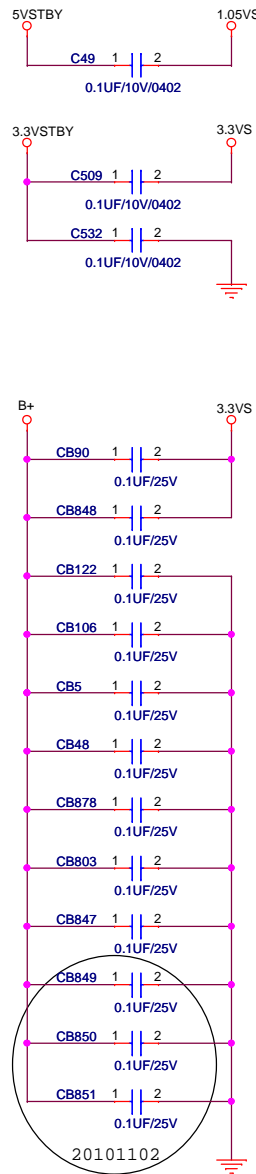
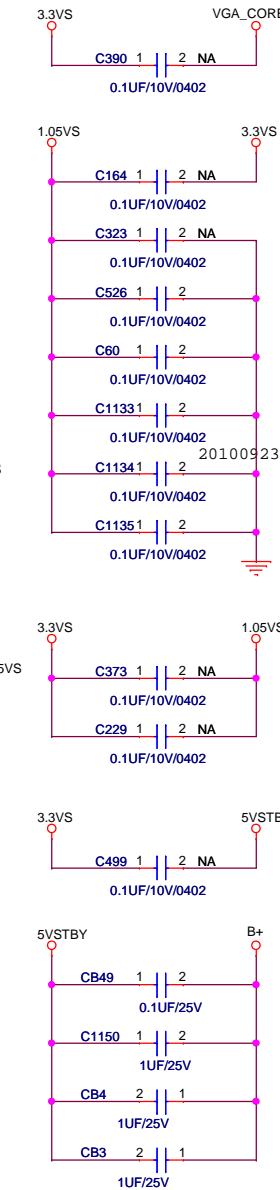
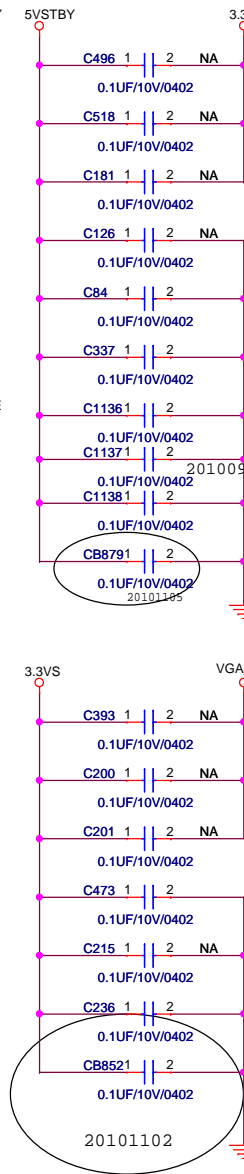
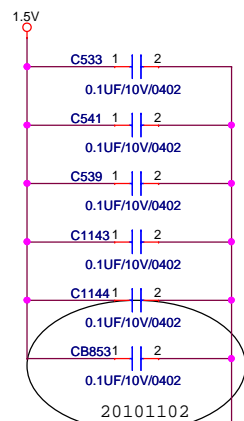
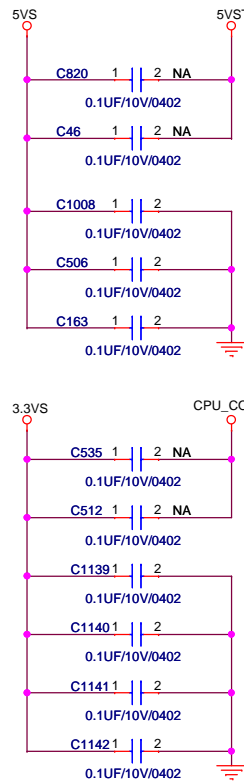
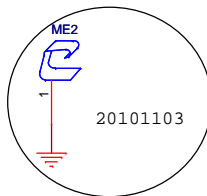
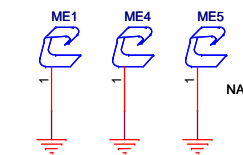
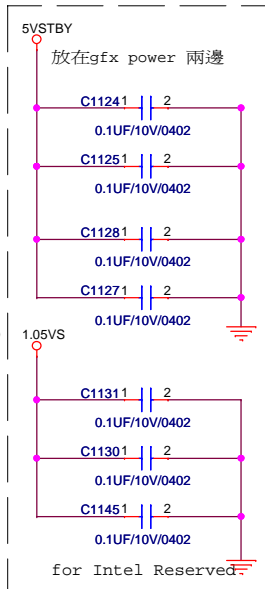
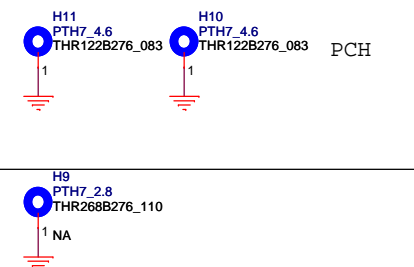
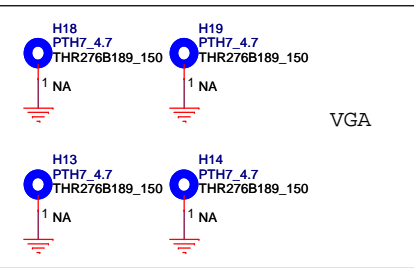
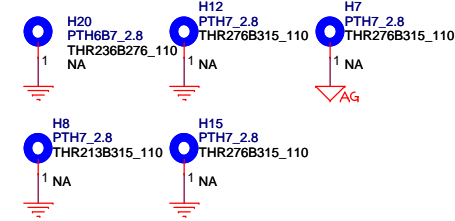
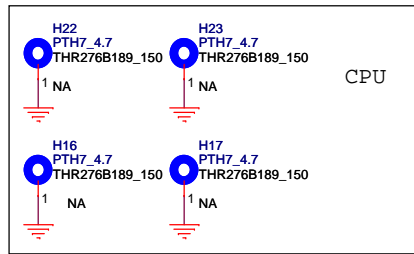
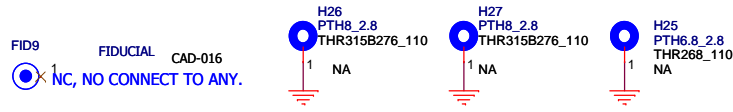


|     |       |     |
|-----|-------|-----|
|     | 15W   | 15W |
| TDC | 15A   | 35A |
| OCF | 22.5A | 50A |



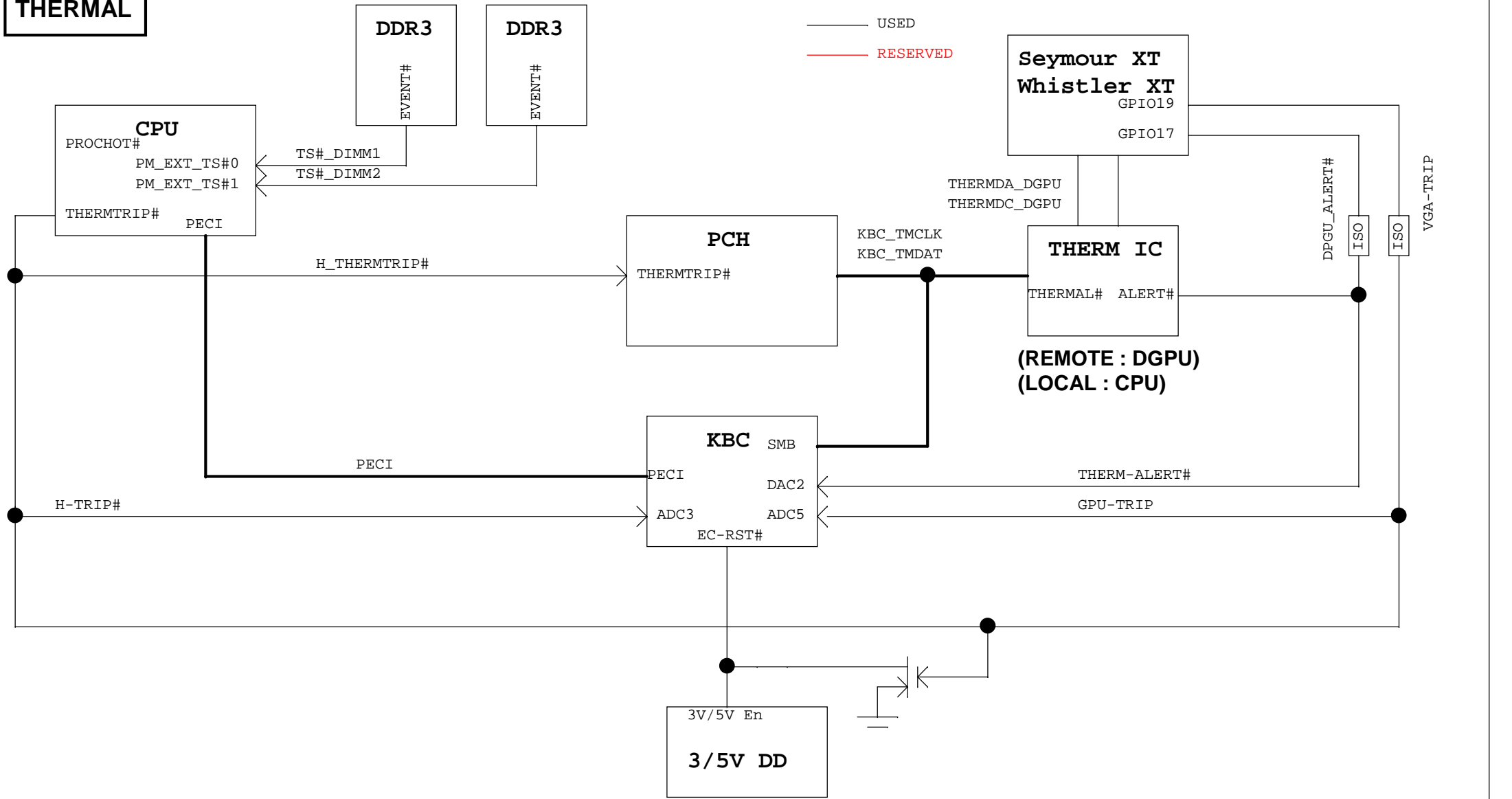
| Seymour GDDR5 (15W) |          |
|---------------------|----------|
| VID0                | VGA_CORE |
| 0                   | 0.9      |
| 1                   | 1.1      |

| FLEX Computing                  |                                      |
|---------------------------------|--------------------------------------|
| Project Name: H710D11           | Title: VGA_CORE(TPS51728)35W         |
| Size: Custom                    | Document Number: HPMH-40GAB6600-B130 |
| Date: Monday, November 08, 2010 | Rev: 8                               |
| Sheet: 57                       | of 63                                |

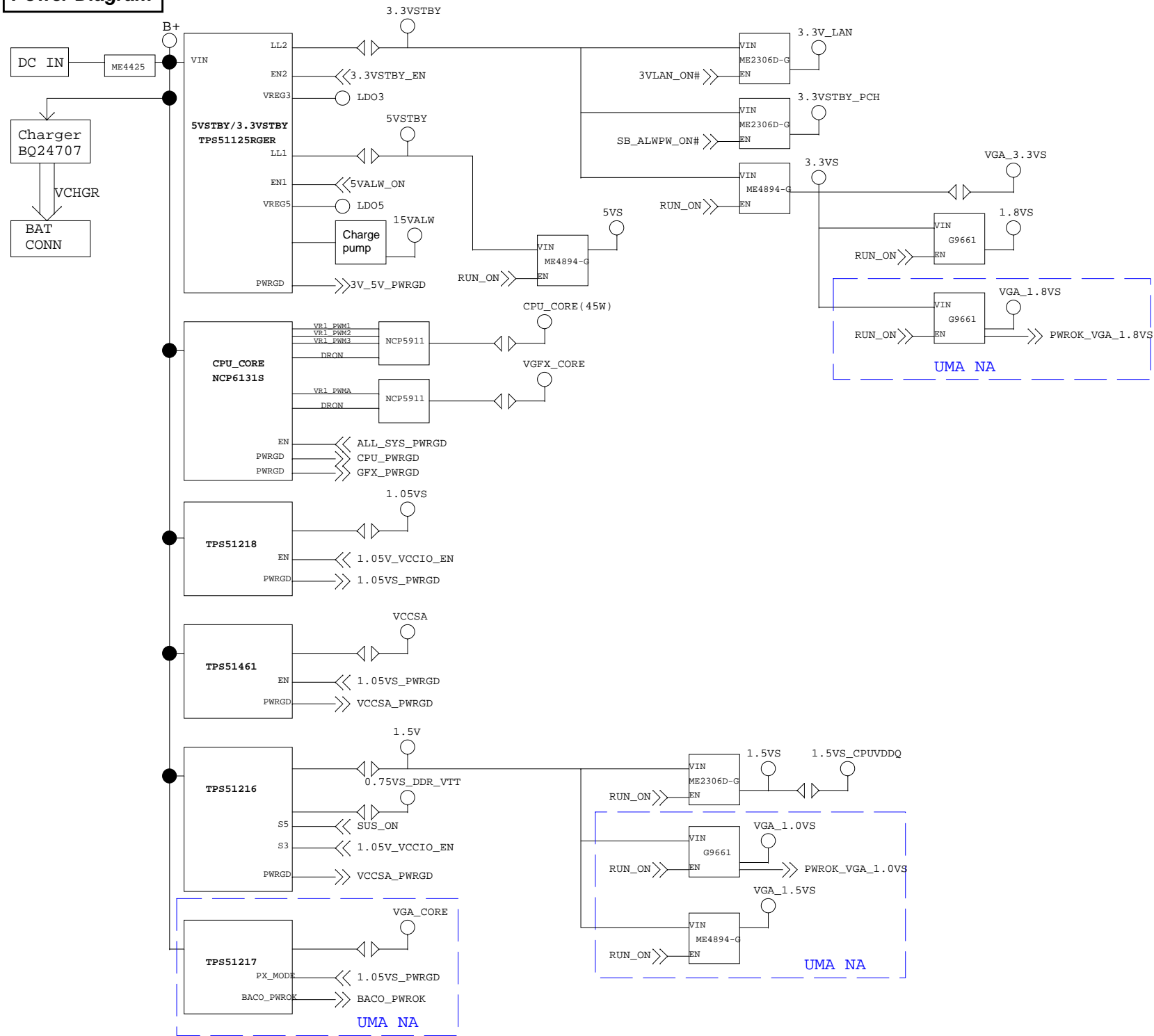


|                                 |  |                                |            |
|---------------------------------|--|--------------------------------|------------|
| FLEXComputing                   |  |                                |            |
| Project Name :<br>H710DI1       |  | Title :<br>PAD_SCREW_ Moat Cap |            |
| Size :                          | Document Number :<br>HPMH-40GAB6600-B130 |                                | Rev :<br>B |
| Date: Monday, November 08, 2010 |  | Sheet: 58 of 63                |            |

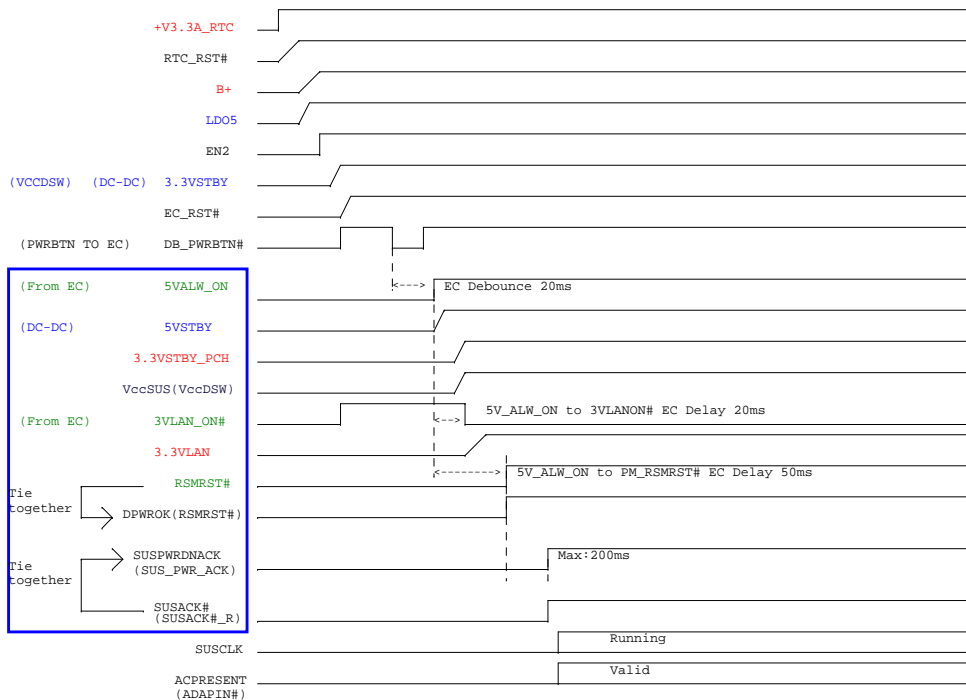
THERMAL



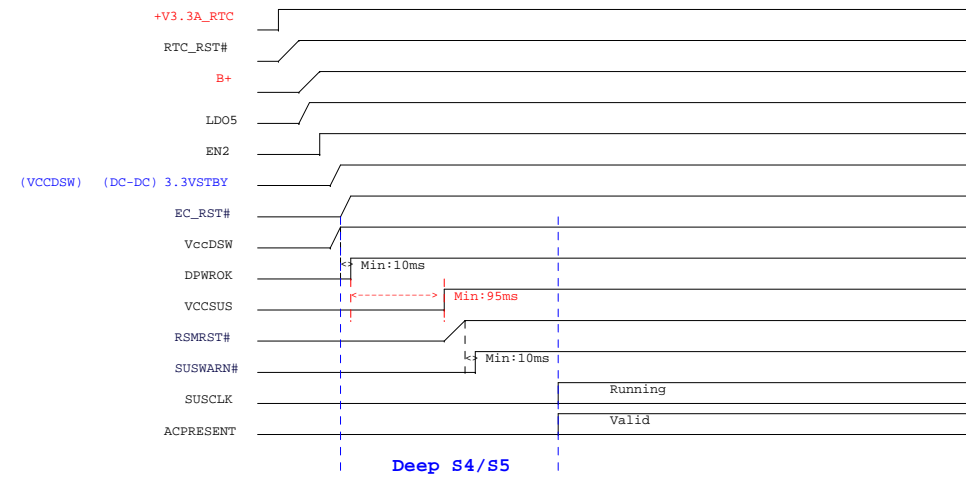
### Power Diagram



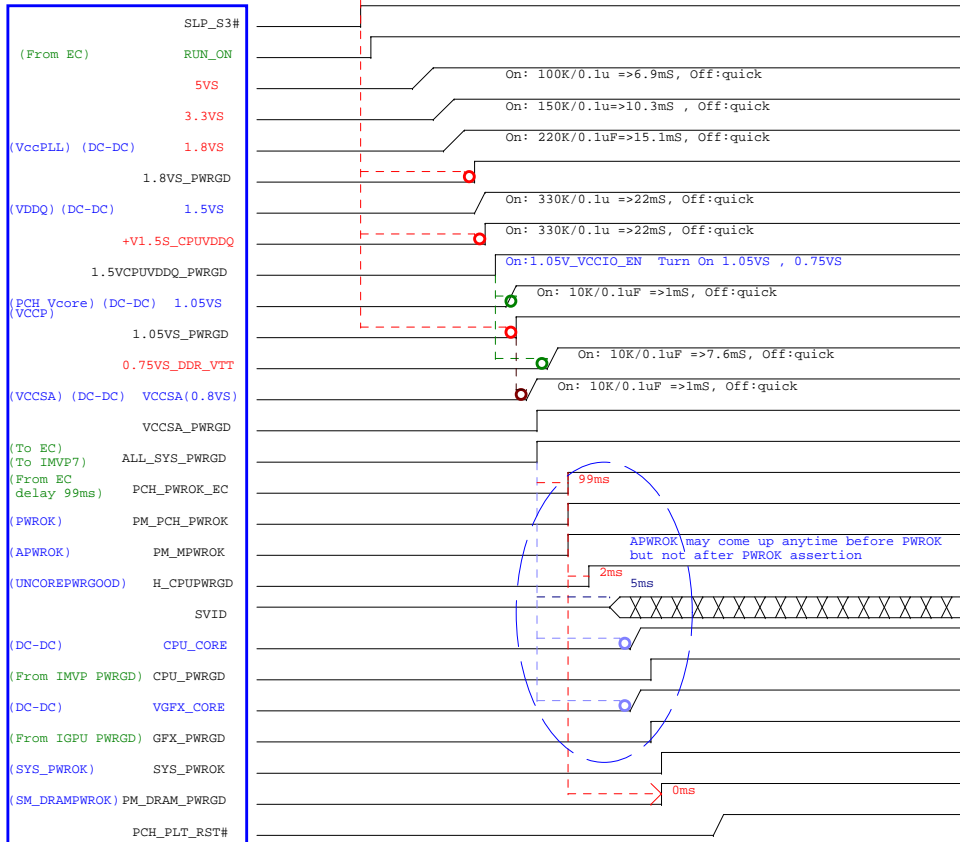
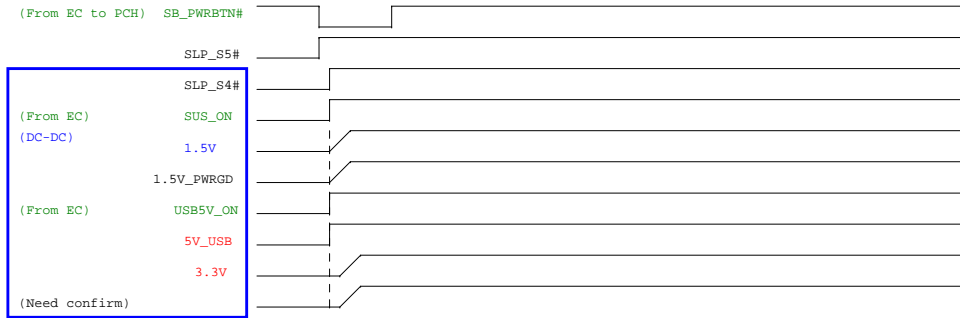
## G3 to S0 (without Deep S4/S5)



## G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT

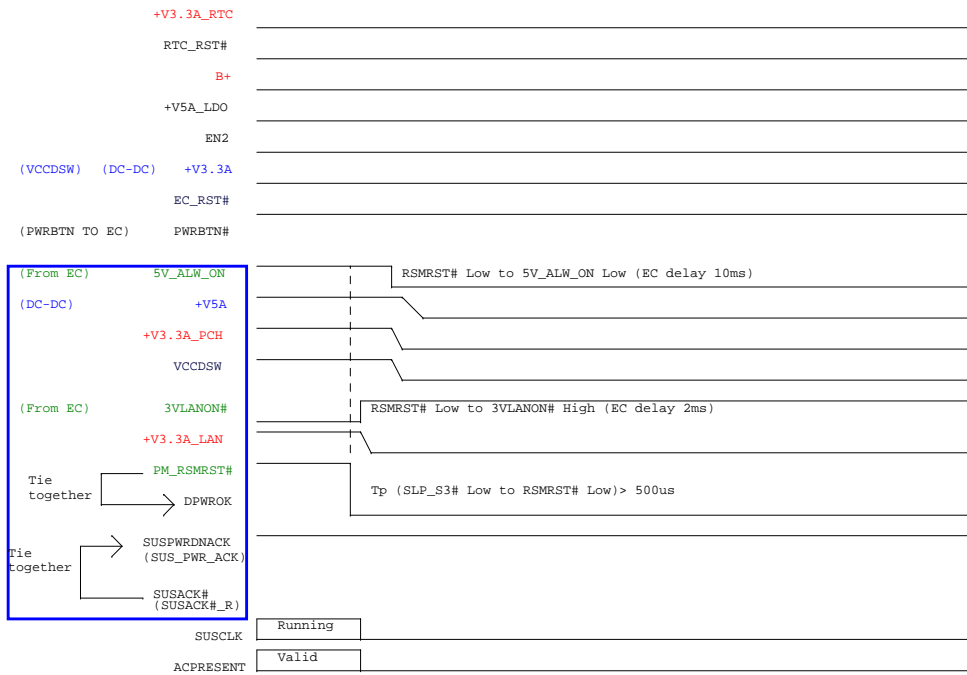


## S5 to S0

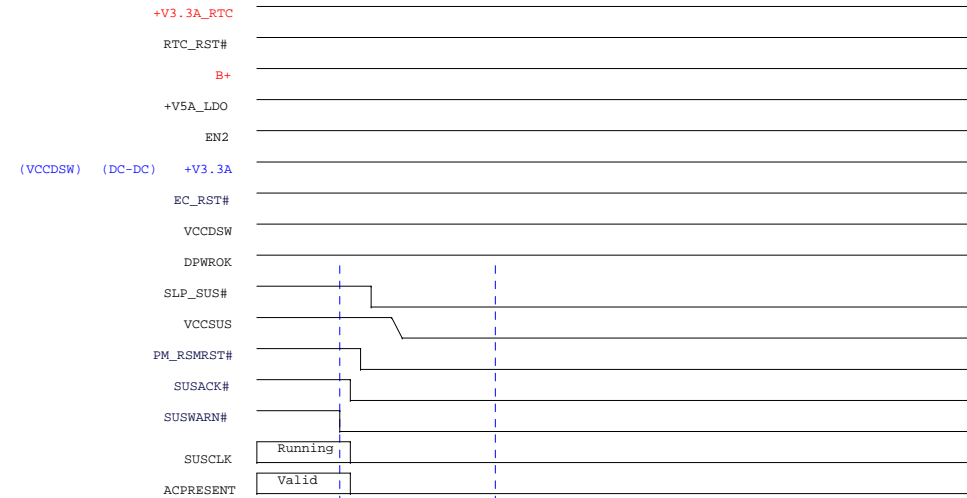


Blue: PWM  
Green: EC  
RED: MOSFET or Others

# S0 to S5 (WoLAN Disable) (without Deep S4/S5)



# S0 to S5 (support Deep S4/S5)



# S0 to S4/S5

